SkyWater SKY130 PDK Documentation

Release 0.0.0-369-g7198cf6

SkyWater PDK Authors

May 29, 2023

CONTENTS

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CURRENT STATUS

> **Warning:** Google and SkyWater are currently treating the current content as an **experimental preview / alpha release**.

While the SKY130 process node and the PDK from which this open source release was derived have been used to create many designs that have been successfully manufactured commercially in significant quantities, the open source PDK is not intended to be used for production settings at this current time. It *should* be usable for doing test chips and initial design verification (but this is not guaranteed).

Google, SkyWater and our partners are currently doing internal validation and test designs, including silicon validation or the released data and plan to publish these results.

The PDK will be tagged with a production version when ready to do production design, see the "*Versioning Information*" section for a full description of the version numbering scheme.

To get notified about future new releases of the PDK, and other important news, please sign up on the skywater-pdk-announce mailing list [join link].

TWO

VERSION NUMBER FORMAT

Version numbers for both the PDK and the supplied libraries are fully specified by a 3-digit version number followed by a git commit count and a git commit short hash.

The 3-digit-number will be tagged in the associated git repository as `vX.Y.Z` and the fully specified value can be found by running `git describe` tool inside the correct git repository.

The version number is broken down as `vX.Y.Z-AAA-gHHHHH`;

- The letter `v`.

- `X` = The "Milestone Release" Number

    - **0** indicates **"alpha"** level. The IP has **not** undergone full qualification. Parts of the IP **may be immature and untested**.

    - **1** indicates **"beta"** level. The IP has undergone qualification testing but has **not** been hardware verified.

    - **2** indicates **production** level. The IP has passed qualification testing and has been hardware verified.

- `Y` = The "Major Release" Number

- `Z` = The "Minor Release" Number

- A single hyphen character –

- `AAA` = The git commit count since the version number was tagged.

- A single hyphen character followed by the letter g `-g`

- `HHHH` = A git commit short hash which uniquely identifies a specific git commit inside the associated git repository.

CURRENT STATUS – EXPERIMENTAL PREVIEW

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KNOWN ISSUES

This section of the documentation provides a list of currently known issues in the currently released files.

See also the SkyWater PDK GitHub issue list to see the latest reported issues.

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4.1 Documentation

A number of sections in the documentation still have pending TODO items. These will be fixed over the coming months.

The current cell datasheets only include basic information about the cell. These datasheets will be continuously updated with new information as the generator is improved.

4.2 PDK Contents Issues

4.2.1 Tooling Compatibility

Cadence Virtuoso Support

The first publication of this is missing files required for optimal Cadence Virtuoso usage. These files will be released publicly at a future date after further work (see Issue #1).

These files are;

- OpenAccess versions of the cells
- Cadence PCells, including
    - Parameterized primitives including FETs, Capacitors, Resistors, Inductors, etc
    - Seal Ring
- Cadence SKILL scripts that support Virtuoso functions such as netlisting

Before these files are released access to the manually created previous version of these files is available through Sky-Water directly under NDA.

Mentor Calibre Support

The first publication of this PDK is missing files required to do design verification with Mentor Calibre. Scripts for generating these files from the published documentation will be released at a future date (see Issue #2).

This includes;

- Physical checking of design rules
- Logic vs schematic checks
- Latchup and soft design rules
- Fill structure generator

Before the scripts are released which generated the needed files for Mentor Calibre from the release documentation, manually created files which provide similar functionality are available from SkyWater directly under NDA.

4.3 Specific Libraries

4.3.1 sky130_fd_pr_base

See *Cadence Virtuoso Support* section.

4.3.2 sky130_fd_pr_rf

The sky130_fd_pr_rf library is provided for references purposes only, all new designs should be based on the sky130_fd_pr_rf2 library.

See *Cadence Virtuoso Support* section.

4.3.3 sky130_fd_pr_rf2

See *Cadence Virtuoso Support* section.

4.3.4 sky130_osu_sc - SKY130 Oklahoma State University provided standard cell library

The SKY130 Oklahoma State University provided standard cells library is currently empty, only a placeholder is currently provided.

The SKY130 Oklahoma State University provided standard cells library will be integrated at a future date (see Issue #10).

4.3.5 sky130_fd_sp_flash - SKY130 Flash Build Space

The flash build space is currently empty, only a placeholder is currently provided.

The components of the SRAM build space compatible with OpenRAM will be released at a future date (see Issue #4).

4.3.6 sky130_fd_sp_sram - SKY130 SRAM Build Space

The flash build space is currently empty, only a placeholder is currently provided.

The components of SRAM build space will be released at a future date (see Issue #3).

4.3.7 sky130_fd_io - SKY130 Foundry Provided IO Cells

The IO cell library is currently empty, only a placeholder is currently provided.

The IO cell library will be released at a future date (see Issue #5).

4.3.8 sky130_ef_io - SKY130 eFabless Provided IO Cells

The IO cell library is currently empty, only a placeholder is currently provided.

The IO cell library will be released at a future date (see Issue #9).

4.4 Design Rule Checking

4.4.1 Using Mentor Calibre

See *Mentor Calibre Support* section.

At the moment, if you are required to use Calibre as part of your design flow, it is recommended that you also use the open source tool Magic to check for errors and fix any issues reported.

4.4.2 Using Magic

Currently Magic does not have DRC checking rules for checking the specialized exceptions for SRAM cells in the sky130_fd_sp_sram SKY130 SRAM Build Space. These will be released at around the same time as the SKY130 SRAM Build Space.

4.5 Scripts and PDK Tooling

A number of scripts are used to generate various files in the PDK including many of the liberty, spice files, schematic images, and much more.

These scripts will be published inside the PDK at a future date (see Issue list).

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SKYWATER SKY130 PROCESS DESIGN RULES

5.1 Background

SKY130 is a mature 180nm-130nm hybrid technology developed by Cypress Semiconductor that has been used for many production parts. SKY130 is now available as a foundry technology through SkyWater Technology Foundry.

The technology is the 8th generation SONOS technology node (130nm).

The technology stack consists of;

- 5 levels of metal (*p* - penta)

- Inductor or Inductor-Capable (*i*)

- Poly resistor (*r*)

- SONOS shrunken cell (*s*)

- Supports 10V regulated supply (*10R*)

5.2 Masks

The `masks.csv file` provides a raw information for the mask layers (name, acronym, usage) currently used found on 130nm processes at SkyWater.

The masks which are used on the SKY130 technology node (that this PDK supports) are marked.

Table 5.1: Table - Masks

Mask	Acronym	Used in SKY130
Field Oxide	FOM	X
Deep N-Well	DNM	X
P-Well Block Mask	PWBM	
P-Well Drain Extended	PWDEM	
N-Well*	NWM	X
High Vt PCh*	HVTPM	X
Low Vt Nch*	LVTNM	X
HLow VT PCh Radio*	HVTRM	X
N-Core Implant	NCM	
Tunnel Mask	TUNM	X
ONO Mask	ONOM	X

Table 5.1 – continued from previous page

Mask	Acronym	Used in SKY130
Low Voltage Oxide	LVOM	X
Resistor Protect	RPM	X
Poly 1	P1M	X
N-tip Implant	NTM	X
High Volt. N-tip	HVNTM	X
Lightly Doped N-tip	LDNTM	X
Nitride Poly Cut	NPCM	X
P+ Implant	PSDM	X
N+ Implant	NSDM	X
Local Intr Cont.1	LICM1	X
Local Intrcnct 1	LI1M	X
Contact	CTM1	X
Open Frame Mask	OFM	
Metal 1	MM1	X
Via	VIM	X
Capacitor MiM	CAPM	
Metal 2	MM2	X
Via 2-TNV	VIM2	
Via 2-S8TM	VIM2	
Via 2-PLM	VIM2	X
Metal 3-TLM	MM3	
Metal 3-S8TM	MM3	
Metal 3-PLM	MM3	X
Pad Via	VIPDM	
Via3-PLM	VIM3	X
Inductor-TLM	INDM	
Metal 4	MM4	X
Via4	VIM4	X
Metal 5	MM5	X
Nitride Seal Mask	NSM	X
Pad (scribe protect)	PDM	X
Pad (scribe unprotect)	PDM	
Polyimide	PMM	
Polyimide_ExtFab	PMM[E]	
Pad&Polyimide_ExtFab	PDMM[E]	
DECA PBO	PBO	X
Cu Inductor/Redist.	CU1M	X
Polyimide 2 (2)	PMM2	X
Under Bump Metal	UBM	
Bumps	BUMP	

5.3 Criteria & Assumptions

5.3.1 Process Stack Diagram

(Diagram not to scale!)
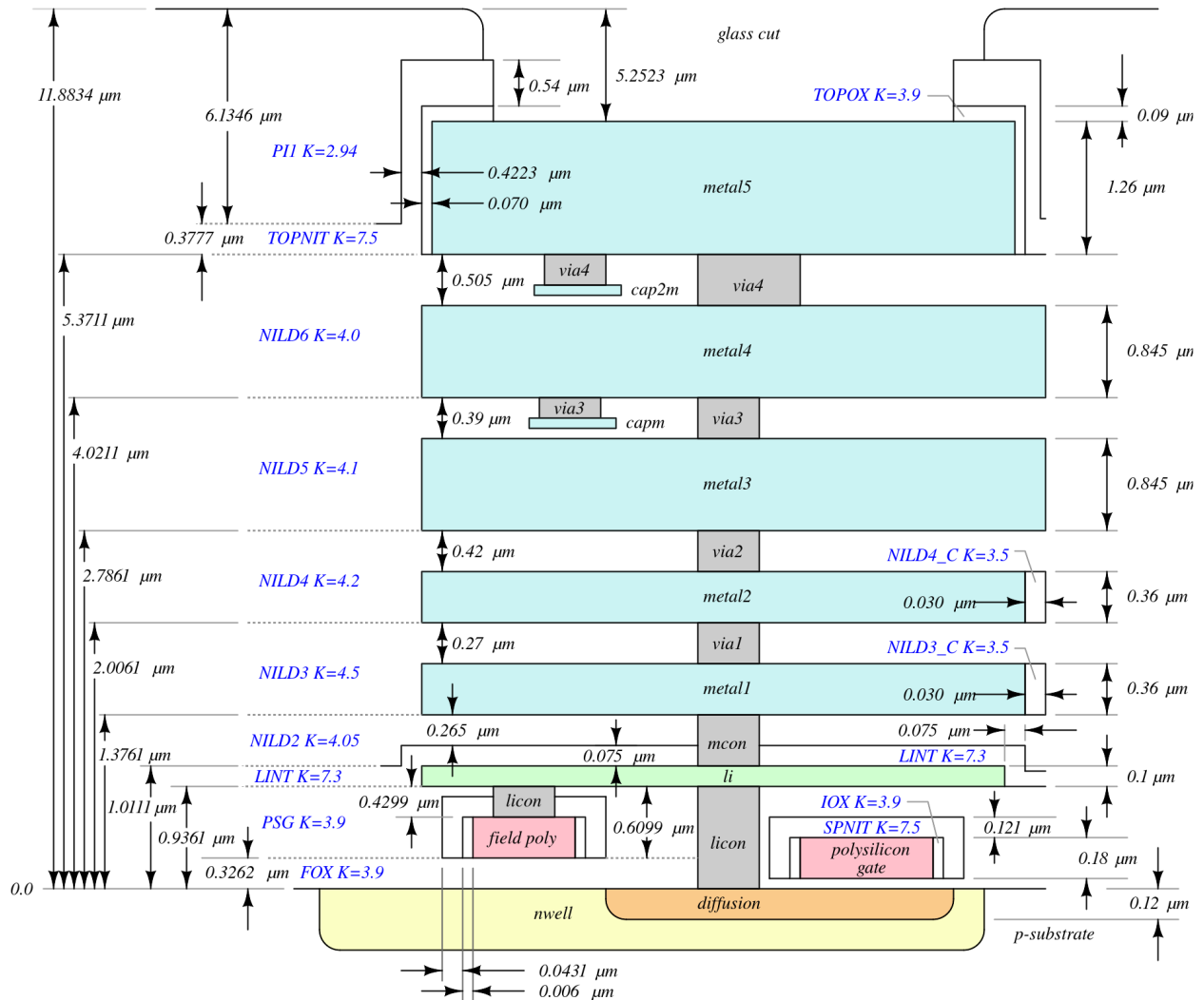
Details about the layers can be found in SkyWater GDS Layers Information page.

5.3.2 General

Table 5.2: Table 1 - General

Parameter	Units	Value	Variable name
Space to Draw		S8	
Grid Size - Drawn	um	0.005	GSF
Approximate Scale Factor for R32 data		0.3	sfr32

5.3.3 Minimum Critical Dimensions

Table 5.3: Table 2 - Minimum CDs in Design or on Wafer, required by Technology (Core or Periphery)

Layer Name		Feature Size	Space Size	Feature Name	Space Name
Field Oxide		0.14	0.27	FOMCD	FOMCDSP
Deep N-Well		3	6.3	DNMCD	DNM-CDSP
P-Well Block Mask		0.84	1.27	PWBMCD	PWBM-CDSP
P-Well Drain Extended		0.84	1.27	PWDEMCD	PWDEM-CDSP
N-Well		0.84	1.27	NWMCD	NWM-CDSP
High Vt PCh		0.38	0.38	HVTPMCD	HVTPM-CDSP
Low Vt Nch		0.38	0.38	LVTN-MCD	LVTNM-CDSP
HLow VT PCh Radio		0.38	0.38	HVTRMCD	HVTRM-CDSP
N-Core Implant		0.38	0.38	NCMCD	NCM-CDSP
Tunnel Mask		0.41	0.5	TUNMCD	TUNM-CDSP
ONO Mask		0.41	0.5	ONOMCD	ONOM-CDSP
Low Voltage Oxide		0.6	0.7	LVOMCD	LVOMCD-SPCSMC
Resistor Protect		1.27	0.84	RPMCD	RPMCDSP
Poly 1	Endcap/Gap	0.15	0.21	P1G	
Poly 1		N/A	0.14	P1MCD	P1MCDSP
N-tip Implant		0.84	0.7	NTMCD	NTM-CDSP
High Volt. N-tip		0.7	0.7	HVNTMCD	HVNTM-CDSP
Lightly Doped N-tip		0.7	0.7	LD-NTMCD	LDNTM-CDSP
Nitride Poly Cut		0.27	0.27	NPCMCD	NPCM-CDSP
P+ Implant		0.38	0.38	PSDMCD	PSDM-CDSP
N+ Implant		0.38	0.38	NSDMCD	NSDM-CDSP
Local Intr Cont.1	Slotted	0.17	0.17	LICM1SLCD	LICM1SLCDSP
Local Intr Cont.1	Core	0.19	0.35	LICM1CD	LICM1CDSP
Local Intrcnct 1	Core	0.14	0.14	LI1MCD	LI1MCDSP
Local Intrcnct 1		0.17	0.17	LI1MCD	LI1MCDSP
Contact		0.17	0.19	CTM1CD	CTM1CDSP
Open Frame Mask		N/A	N/A	OFMCD	OFMCDSP
Metal 1		0.14	0.14	MM1CD	MM1CDSP

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Table 5.3 – continued from previous page

Layer Name		Feature Size	Space Size	Feature Name	Space Name
Metal 1 - Cu		0.14	0.14	MM1_CuCD	MM1_CuCDSP
Via		0.15	0.17	VIMCD	VIMCDSP
Via - Cu		0.18	0.13	VIM_CuCD	VIM_CuCDSP
Capacitor MiM		2	0.84	CAPMCD	CAPM-CDSP
Metal 2		0.14	0.14	MM2CD	MM2CDSP
Metal 2 - Cu		0.14	0.14	MM2_CuCD	MM2_CuCDSP
Via 2-TNV		0.28	0.28	VIM2CD	VIM2CDSP
Via 2-S8TM		0.8	0.8	VIM2CD	VIM2CDSP
Via 2-PLM		0.2	0.2	VIM2CD	VIM2CDSP
Via 2-Cu		0.21	0.18	VIM2_CuCD	VIM2_CuCDSP
Metal 3-TLM		0.36	0.36	MM3CD	MM3CDSP
Metal 3-S8TM		0.8	0.8	MM3CD	MM3CDSP
Metal 3-PLM		0.3	0.3	MM3CD	MM3CDSP
Metal 3-Cu		0.3	0.3	MM3_CuCD	MM3_CuCDSP
Pad Via		1.2	1.27	VIPDMCD	VIPDM-CDSP
Via3-PLM		0.2	0.2	VIM3CD	VIM3CDSP
Via3-Cu		0.21	0.18	VIM3_CuCD	VIM3_CuCDSP
Inductor-TLM		2.5	2.5	INDMCD	INDM-CDSP
Metal 4		0.3	0.3	MM4CD	MM4CDSP
Metal 4-Cu		0.3	0.3	MM4_CuCD	MM4_CuCDSP
Via4		0.8	0.8	VIM4CD	VIM4CDSP
Metal 5	All flows except S8PF*/S8PIR*	0.8	0.8	MM5CD	MM5CDSP
Metal 5	S8PF*/S8PIR*	1.6	1.6	MM5CD	MM5CDSP
Nitride Seal Mask		3	4	NSMCD	NSMCDSP
Pad (scribe protect)		2	1.27	PDMCD	PDMCDSP
Polyimide		5	15	PMMCD	PMM-CDSP
Polyimide_ExtFab		5	15	PMM[E]CD	PMM[E]CDSP
DECA PBO		10	10	PBOCD	PBOCDSP
Cu Inductor/Redist.		20	20	CU1MCD	CU1MCDSP
Serifs		0.1	0.1	SERCD	SERCDSP

5.3.4 Semiconductor Criteria

Basic Parameters

Table 5.4: Table 3a - Semiconductor Criteria - Basic Parameters

	Units	Value	Variable name
n-well peak concentration	cm-3	6.00E+017	NWPCONC
background concentration	cm-3	8.00E+14	NWBCONC
y.char	um	0.43	NWYCHAR
desired Nmin/Ns ratio		0.9	NMINNSRA-TIO
min n-well width to guarantee 90 % peak concentr.	um	0.55	MIN-NWWID
p-well peak concentration	cm-3	4E+017	PWPCONC
p-well peak coordinate	um	0.42	PWPCO-ORD
y.char	um	0.13	PWYCHAR
min. p-well width to guarantee 90 % peak concentr.	um	0.33	MINPWWID

Junction Depths

Table 5.5: Table 3b - Semiconductor Criteria - Junction Depths

	Units	Vertical Feature	Vertical Space	Variable name
Baseline: N-Well	um	1.1		NWVDIM
P-Well	um	0.75		PWVDIM
N-w/P-w junction (from drawn edge)	um	•	0.034	WELLJCT
N+ or P+ S/D (XJ)	um	0.1	0.06	JCTD / LD
Max (N+ or P+ S/D outdiff.) next to isol. edge	um		0.007	LDST
Max (N+ or P+ S/D outdiff.) next to isol. edge for 6 V reg. devices			0.05	LDST5
N Tip (As)	um		0.01	LDNTIP

Other Width Criteria

Table 5.6: Table 3c - Semiconductor Criteria - Other Width Criteria

	Units	Value	Variable name
Min. diff/tap width for reproducible resistivity	um	0.12	MINFWR
Min. width to open a strip of tap between two diffs	um	0.34	SDM3
Max s/d diff width without contact, consistent w/Ram4,5,6	um	5.7	XMAXCON

Punchthrough Criteria

Table 5.7: Table 3d - Semiconductor Criteria - Minimum Spacing for
3.3V Punchthrough (1.8V devices)

	Units	Value	Variable name
n-well - n-well	um	0.835	NWPTS
n+ - n+ or p+-p+	um	0.23	DPTS
p+ in nwell to pwell	um	0.05	PPTS
n+ in pwell to nwell	um	0.15	PNPTS

Latch-up/ESD Criteria

Table 5.8: Table 3e - Semiconductor Criteria - Latch-up/ESD Criteria

	Units	Value	Variable name
Minimum n+ or p+ - nwell spacing to prevent latch-up	um	0.23	NPNWLU
Min n-well enclos. of tap to ensure bkdwn N-w/P-w before N+/P-w (ESD)	um	0.04	XNWESD
Max. overlap of n-well by p+ tap	um	0.06	XNWPTS

Implant angles

Table 5.9: Table 3f - Semiconductor Criteria - Implant angles

	Units	Angle		Variable name
High current	deg	0	0	HCIMPA
Angle for tip implant	deg	7		TipAng
Angle for HV tip implant	deg	40		HvTipAngle
Twist angle for HV Tip	deg	23		HvTipTwist

5.3.5 Physical Criteria

Table 5.10: Table 4 - Physical Criteria

Material Thicknesses	Value (um)	Variable name
field oxide (above silicon surface) … underneath poly	0.07	FOXSTEP
min. etch and fill capability for isolation, licon, and met1	0.15	DEFC
min. etch and fill capability for mcon	0.14	CEFC
min. etch and fill capability for via	0.18	VEFC
poly cap after SPE	0.2	OVGTTH
poly thickness	0.18	POLYTH
oxide spacer	0.05	SpThickn

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Table 5.10 – continued from previous page

Material Thicknesses	Value (um)	Variable name
Pre-LI ILD thickness	0.5	ILDTHICKN
Licon1 etch angle (deg)	10	LIC-ETANG
Standard Licon bottom CD	0.08	LBCD
Mcon enclosure by Li	0	mcon-LiEn-closure
Via1 slope	0.02	Via1Slope
Oxide Bias for MM1	0.6	Bi-asMM1
Oxide Bias for MM2	0.6	Bi-asMM2
Oxide Bias for MM3	1.15	Bi-asMM3
Oxide Bias for MM4	1.15	Bi-asMM4
LI1 thickness for antenna ratio calculations	0.1	LiThick
Metal 1 thickness for antenna ratio calculations (S8D*)	0.35	Met1Thick
Metal 2 thickness for antenna ratio calculations (S8D*)	0.35	Met2Thick
Inductor thickness for antenna ratio calculation (S8D*)	4	In-dmThick
Metal 3 thickness for antenna ratio calculation (S8Q/SP8Q)	0.8	Met3thick_q
Metal4 thickness for antenna ratio calculation (S8Q*/SP8Q)	2	Met4Thick_q
Metal 3 thickness for antenna ratio calculation (S8P*/SP8P*)	0.8	Met3thick_p
Metal4 thickness for antenna ratio calculation (S8P*/SP8P*)	0.8	Met4Thick_p
Metal5 thickness for antenna ratio calculation (S8P*/SP8P* with 2um thick metal)	2	Met5Thick_p
Metal5 thickness for antenna ratio calculation (S8P*/SP8P* with 1.2um thick metal)	1.2	Met5Thickp_12
Metal 2 thickness for antenna ratio calculations (SP8T/S8T*)	0.35	Met2_Qthick
Metal 3 thickness for antenna ratio calculations (S8T* other than S8TM*)	0.85	Met3_Qthick
Metal 3 thickness for antenna ratio calculations (S8TM* flow)	2	Met3_TMthick
Metal 3 thickness for antenna ratio calculations (SP8T flow)	0.8	Met3_SP8Tthick
Photoresist thickness	1.14	PRTHICKN
Photoresist thickness for HV Tip Implants	0.3	PrThickIm-plant
Min width of tip implant opening	0.1	minTip_impW
NTM shadowing	0.16	ntmShad-owing
HVNTM shadowing	0.232	hvntmShad-owing
HVPTM shadowing	0.089	hvptmShad-owing
pseudo-shadowing	0.045	pseu-doShad-owing

Table 5.10 – continued from previous page

Material Thicknesses	Value (um)	Variable name
Channel length for low Vt PMOS	0.35	lvtpmos_poly
Width of the Low Leakage gate on each side of LowVt Pmos connected to power rails (requirement based on exp data)	0.28	LvtEnc_forPowerRail
CD tolerance for PDM (3s)	1	PdmCD_tol
Min process bias 3s tolerance	0.032	PHTOL
Min process bias 3s tolerance for poly	0.02	PHP1TOL
Minimum Space and Overlap	Value (um)	Variable name
Minimum mcon overlap onto LI for reproducible contact resistance	0.12	TCONOVLP
Dogbone PR decay length (SRS 8/4/99)	0.2	DBPRDEC
Bowing of rectangular contact (per edge) – seal ring sizing	0.015	TBOWINGSEAL
Waffling / Pattern Density	Value	Variable name
S8 average FOM PD (extractions from logic device)	0.45	FOMPDAVG
Size of small PD extraction box for rough tolerance (um)	700	SMALLPDBOX
Size of large PD extraction box for rough tolerance (um)	2000	LARGEPDBOX
Min pattern density for oxide	0.75	OxideMinPD
Min MM* PD range	0.3	MMPDrange
FOM 700um box PD tolerance for CMP (SOI8 PCR2) for all technologies	0.15	FOM700TOL
Stepping box shift as a percent of box size	0.5	BOXSHIFT
Maximum metal waffle drop pattern density in the frame	0.55	PD_FrameWP
Window size for frame waffle drop PD check	100	WP_PDWINDOW
Step size for frame waffle drop PD check	10	WP_PDSTEP
Other	Value	Variable name
Poly resistor width and spacing to reduce CD variation (um)	0.33	POLYRCD
Poly resistor width and spacing to reduce CD variation (um)	0.48	POLYRSPC
Spacing between slotted_licons (Not applicable when the two edges L= 0.19um)	0.51	LICM1SLSP1
Precision resistor width to accommodate 6 contacts across	2.03	PRECRESW
Li resistor width (to drop one Licon w/o dogbones)	0.29	LIRESCD
Correction factor for spacing to a wide metal line	2	BIGMF
Min spacing for created dnwell to pnp.dg (more restrictive than dnwell.4 rule)	5	cdnwPnpSpc
Min spacing between nwell and deep nwell on separate nets (Taken from dnwell.3 from S4* TDR *N plus rounded up, IGK request.)	6	nwellDnwellSpc
Min space between deep nwells used as photo diode (um)	5	PDDnwSpc

Table 5.10 – continued from previous page

Material Thicknesses	Value (um)	Variable name
Min space between dnwell (used for photo diode and other deep nwell (um)	5.3	PDDnwSpc1
Min/Max width of nwell inside deep nwell (for photo diodes)	0.84	PDNwmCD
Min/Max enclosure of nwell by deep nwell (for photo diode)	1.08	PDNwmD-nwEnc
Min/Max width of tap inside deep nwell (for photo diode)	0.41	PDTapCD
Min/Max enclosure of tap by nwell inside deep nwell (for photo diode)	0.215	PDTap-N-wmEnc

5.3.6 Laser Fuse Criteria

Table 5.11: Table 5 - Laser Fuse Criteria

	Value (um)	Variable name
Min. spac. of laser spot to diffused junction to ensure jct integrity	0.6	XLASJUN
Max. width of a metal fuse line that can be removed reliably	0.8	FSW
Min. L of met. fuse at which damage doesn't extend beyond ends	6.605	FSLE
Max. extension of met2 beyond fuse boundary	0.005	FEXT
Min. distance between laser spot and active junction	0.545	LASJCT
Standard contact bottom CD	0.09	
Positioning tolerance of laser spot (3 s)	0.3	LASMA
Nominal effective laser spot diameter	3.5	LASSPT
Max. increase in spot diameter at max. distance from focus (3 s)	0.9	LASCD-TOL
Fuse melting radius	3.6	MELTRAD
Melting related crack size in ILD	0.36	FUSE-CRACK
Min space between fuse and any feature not connected to it	0.2	MinFus-eSpace
Space between fuse and any unrelated layer	0.5	SP_fuse_to_unrelated
DC offset in some fuse rules	0.87	LASDC1

5.3.7 Other criteria and parameters

Table 5.12: Table 7 - Other criteria and parameters

Layer / Design rule	CD	space	Comment
MOSFET width	0.135		FOMSE
MOSFET width in standard cells	0.075		FOM-SESC

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Table 5.12 – continued from previous page

Layer / Design rule	CD	space	Comment
Spacing of poly on field to diff		0.065	PFDSE
Spacing of poly on field to tap		0.005	PFTSE
Enclosure of tap by nwell for pwell res		0.22	PTAP_NWL_SP
Grid conversion rounding factor		0.005	GRCF
Licon enclosure rounding		0.02	LICEN-CLR
LI1CD add/drop	0.01	0.04	
Huge metal X min. W and L	3		HugeM
Min Nsdm area	0.265		MinNs-dmArea
Min Psdm area	0.255		MinPsd-mArea
Min N/Psdm hole area	0.265		Min-NPsdm-Hole
Large waffle size must be divisible by 4	7.2		waf-fle_large
P1M additional CD control	0.011		P1MCDcontrol
Li1 proximity correction		0.25	LI1PROXSpace
Serif added to nwell convex corner (SXX-572, 573)	0.22		Nwell-CvxSerif
Serif added to nwell concave corner (SXX-572, 573)	0.12		Nwell-CveSerif
NWM extension beyond nwell edge straddling de_nFet_source (for GSMC; QZM-133)	0.075		NvhvN-wellExt
Min enclosure of pad by pmm for Cu inductor (JNET-80)	0		padPM-MEncInd
Min enclosure of pmm by cu1m for Cu inductor (JNET-80)	10.75		pmmCu1mEncInd
Min enclosure of pbo by cu1m per DECA 000348 Rev S	10		pboCu1mEnc
Min enclosure of pmm by pmm2 for radio flow in the die (JNET-80)	13		pmmPmm2EncInd
Min enclosure of pmm by pmm2 inside frame	7.5		pmmPmm2EncIndFrame
Min space between pmm2 and Inductor.dg		7.5	pmm2IndSpc
Min cu1m PD across full chip	0.35		MinCU1Mpd
Max cu1m PD across full chip	0.45		MaxCU1Mpd
Spacing between RDL and outer edge of seal ring	15		RdlSeal-Spc
Spacing between RDL and pmm2	6.16		RdlPmm2Spc
Enclosure of etest module in die by cpmm2	0		EtestCpmm2Enc
Keepout of active, poly, li and metal to NSM (TCS-2253)		1	NSM-Keepout
3 um keepout of active, poly, li and metal to areaid.dt/areaid.ft (TCS-2253)		3	NSM-Keep-out_3um
pnp_emitter sizing (S8P GSMC flow)		0.05	Pn-pEmit-ter-SzGSMC

continues on next page

Table 5.12 – continued from previous page

Layer / Design rule	CD	space	Comment
pnp_emitter sizing (other flows)		0.03	PnpEmitterSz
MiM Capacitor aspect ration	20		MiM_AR
Min NCM space to be used to preserve NCM CL algorithm (avoid LVL error)		1.27	NCM_0LVL
Min space of NCM between core and periphery due to existing layout restriction		0.96	NcmCorePeriSP
Multiplication factor		0.01	S8LVconv
Minimum scribe width	50		scribew
spacing of p-well outside deep n-well to deep n-well mask edge		0.12	NWD-NWENCL
p-well in deep n-well to p-sub		1.2	NWD-NWOL
Field oxide etchback after P1ME before implants		0.04	WFDEL

5.3.8 Criteria for High Voltage FET

Table 5.13: Table 8 - Criteria for High Voltage FET

Layer / Design rule	CD	space	Comment
Min HVNwell to any nwell space		2	HVNwell_Nwell_SP
Min HVDiff width	0.29		HVDiff_CD
Min HVDiff space		0.3	HVDiff_SP
Min HV Pmos gate width	0.5		HVP_gate_CD
Min space between HV poly		0.28	HVPoly_SP
Min HV Nmos gate width	0.37		HVPoly_CD
HV P+ Diff enclosure by Nwell	0.33		HVPdiff_nwell_enc
HV N+ diff space to Nwell		0.43	HVNdiff_nwell_SP
HV N+ tap enclosure by Nwell	0.33		HVNtap_nwell_enc
HV P+tap space to Nwell		0.43	HVPtap_nwell_SP
Photoresist tilted implant penetration	0.02		HVPrPenetration
Photoresist tilted implant blocking distance	0.013		HVPrBlocking
Min size of HVTip	0.1		HVTipMinSize
Extra CD tol for HVNTM to match Ram7 process	0.015		HVNTMExtraCdTol
Min HVDiff resistor width	0.29		HVDiff_Res_CD
High voltage n+-n+ or p+-p+		0.3	HVDPTS15
HV MOSFET channel length	0.5		HVPCD

5.3.9 Criteria for polyimide manufacturability

Table 5.14: Table 9 - Criteria for polyimide manufacturability

Layer / Design rule	CD	space	Comment
Enclosure of fuses by polyimide	12		PimFuseEnc
Enclosure of bondpad by polyimide (YUY-165)	0.5		PimPadEnc
Enclosure of pad:dg by PBO inside inductor capture pad, with DECA online monitoring	4.5		PBOPadEnc
Enclosure of pad:dg by PBO per standard DECA rules	7.5		PBOPadEncDECA
DECA PBO drawn-to-final process bias per side	0.5		PBOProcBiasPerSide
Polyimide CD tolerance	1		PimCD_tol
Min Pim width over pad openings	87		PimOverPad_CD
Polyimide slope (001-87400)		5	I_polyimide_slope
Enclosure of polyimide by polymer tolerance		7	Po_po_tol
Min/Max enclosure of pad.dg inside M5RDL by pmm	0		pmmM5RDLpadEnc
Min spacing of pmm to (rdl NOT (pad.dg sized by 0.5))		19.16	pmmRDLspc
Enclosure of laser targets in the die by polyimide	30		PimLaserEnc

5.3.10 Criteria for VPP capacitor

Table 5.15: Table 10 - Criteria for VPP capacitor

Layer / Design rule	CD	space	Comment
Min width of capacitor:dg	4.38		VppWidth
Max width of unit capacitor:dg	8.58		VppMaxWidth
Min spacing between two capacitor:dg	1.5		VppSpc
Min spacing of capacitor:dg to li1 or met1 or met2 or nwell	1.5		VppOtherSPc
Min enclosure of capacitor by nwell	1.5		VppNwmEnc
Min spacing of pmm to (rdl NOT (pad.dg sized by 0.5))		19.16	pmmRDLspc

5.4 Layers Reference

5.4.1 Layers Definitions

Table 5.16: Table C3: Dev

Name	Defining algorithm
AR_met2_A	Net Area Ratio of met2 not connected to via and of via2 >=0.05 [Equation: (AREA(via2))/(2 * AREA
AR_met2_B	Net Area Ratio of met2GroundOrFloat, via, and via2 <=0.032 [Equation: (AREA(via2))/(2 * AREA(n
bondPad	pad:dg OUTSIDE areaid:ft
bottom_plate	(capm:dg AND met2:dg) sized by capm.3; Exclude all capm sharing same metal2 plate
Capacitor	Capm enclosing at least one via2
Chip_extent	Holes (areaid:sl) OR areaid.sl
Diecut_pmm	areaid.dt NOT (cfom.wp OR cp1m.wp OR cmm1.wp OR cmm2.wp)
drain_diffusion	(diff NOT poly in nwell or pwell) not abutting tap in the same well or abutting tap in the opposite well
dummy_capacitor	Capm not overlapping via2
dummy_poly	poly overlapping text "dummy_poly" (written using text.dg)
ESD_nwell_tap	n+ tap coincident with nwell such that n+ tap and nwell are completely surrounded by and abutting n+
fomDmy_keepout_1	(diff.dg OR tap.dg OR poly.dg OR pwell resistor OR pad OR cfom.dg OR cfom.mk OR PhotoArray O
floating_met*	met*.dg not connected to diffusion or tap through met(*+1) or met(*-1)* and their respecitve vias and con
fom_waffles	fom.mk with dimensions (um x um): 0.5 x 0.5, 1.5 x 1.5, 2.5 x 2.5 and 4.08 x 4.08
gated_npn	cell name: s8rf_npn_1x1_2p0_HV
huge_metX	Metal X geometry wider and longer than 3.000um
hugePad	pad.mk with width > 100um
iso_pwell	(NOT nwell) AND dnwell
isolated_tap	tap that does not abut diff
laser_target	cell *lazX_* and *lazY_* OUTSIDE areaid:ft
LVnwell	nwell NOT hvi
LVTN_Gate	Gate overlapping lvtn
met2GroundOrFloat	met2 connected to ptap or met2 not connected to difftapn
met2GroundOrFloatVia	met2GroundOrFloat interacting with via2 >2
N+_diff	Diff NOT Nwell
N+_tap	Tap AND Nwell
nsdmHoles	Hole(nsdm)
NSM_keepout	nsm.dg OR nsm.mk
nwell_all	nwell OR extension of cnwm beyond nwell edge straddling de_nFet_source by cnwm.3f (45 degree edg
P+_diff	Diff AND Nwell
P+_tap	Tap NOT Nwell
Pattern_density	(diff_tap area) / PD window (as specified in the rule section)
photoDiode	deep nwell overlapping areaid.po. Die+frame utility will use the mask data of dnwell in the implementa
poly_licon1	Any licon1 that does not overlap ((diff or tap) NOT poly)
poly_waffles	p1m.mk with dimensions (um x um): 0.48 x 0.48, 0.54 x 0.54 and 0.72 x 0.72
prec_resistor	rpm AND (poly overlapping poly.rs) AND psdm
prec_resistor_terminal	prec_resistor AND li
psdmHoles	Hole(psdm)
pwell	NOT nwell (default substrate area)
pwres_terminal	P+tap abutting pwell.rs
pnp_emitter	diff AND pnp.dg AND psdm
routing_terminal	metX.pin sized inside of metX.drawing by 1/2 * metalX min width; Similar defintion applies to Li1 lay
scribe_line	areaid:ft NOT areaid:dt
slotted_licon	licon1.dg of size 0.19um x 2.0um

Table 5.16 – cont

Name	Defining algorithm
slotted_licon_edge1	2.0um edge of the slotted_licon
source_diffusion	(diff NOT poly in nwell or pwell) abutting tap in same well
tap_licon	Tap AND Licon1
tap_notPoly	tap NOT poly
top_indmMetal	met3 for S8D*
top_metal	met3.dg OR mm3.mk (for S8T*/SP8TEE-5R); met3.dg OR indm.mk (for S8D*); met4.dg OR mm4.m
top_padVia	Via2 for S8D*
top_plate	capm:dg
Var_channel	poly AND tap AND (nwell NOT hvi) NOT areaid.ce
VaracTap	Tap overlapping Var_channel
vpp_with_noLi	vpp with cell names: FIXME
vpp_with_Met3Shield	vpp with cell names: FIXME
vpp_with_LiShield	vpp with cell names: FIXME
vpp_over_MOSCAP	vpp with cell names: FIXME when over nhvnative W/L=10x4, FIXME when over phv/pshort/phighvt/
vpp_with_Met5PolyShield	vpp with cell names: FIXME
vpp_with_Met5	vpp with cell names: FIXME
cp1m_HV	cp1m AND Hvi
de_nFet_drain	((isolated tap) AND areaid.en) overlapping nwell
de_nFET_gate	deFET_gate overlapping (diff NOT dnwell)
de_nFet_source	(diff AND areaid.en) overlapping de_nFET_gate
de_pFet_drain	((isolated tap) AND areaid.en) not overlapping nwell
de_pFET_gate	deFET_gate overlapping (diff AND dnwell)
de_pFet_source	(diff AND areaid.en) overlapping de_pFET_gate
deFET_gate	(poly AND areaid.en) not overlapping pwm ; For CAD flows that do not have pwm layer, it is (poly AN
Hdiff	Diffusion AND Hvi
Hgate	Hpoly AND diff
Hnwell	Nwell AND Hvi
Hpoly	Poly AND Hvi
Htap	Tap AND Hvi
hv_source/drain	= (diff andNot poly) that overlaps diff.hv
hvFET_gate	= FET_gate butting hv_source/drain
hvPoly	= poly electrically connected to hv_source/drain
HV_nwell	(nwell AND hvi) OR (nwell overlapping areaid.hl)
stack_hv_lv_diff	(diff And Hvi NOT nwell) abutting (diff NOT nwell)
SHVdiff	Diff And shvi
SHVGate	SHVPoly AND diff
SHVPoly	Poly OVERLAP shvi:dg
SHVSourceDrain	Diff And shvi NOT poly NOT diff:rs
VHVdiff	Diff And vhvi
VHVGate	VHVPoly AND diff
VHVPoly	Poly OVERLAP vhvi:dg
VHVSourceDrain	(Diff AND tap) And vhvi NOT poly NOT diff:rs
background	Area where waffling grid is defined, sized to avoid waffle shift between runs
die	Holes (areaid:sl)
frame	(areaid.ft SIZE by -(max of s.2e/h)) NOT (OR areaid.dt SEALIDandHole)
inductor_metal	(inductor:dg AND (met1 OR met2 OR met3)) size by 10 um [For all flows except S8PIR-10R]ninducto
mm*_slot	mm* slots are defined as empty holes in metal that are located in (areaid.cr OR areaid.cd)
nwellDnwellHoles	(inner HOLES of nwellAndDnwell). Die+frame utility will use the mask data of nwell and dnwell in th
photoArray	(OR nwellAndDnwell nwellDnwellHoles) enclosing photoDiode. Die+frame utility will use the mask o
gate	poly AND diff

Table 5.16 – con

Name	Defining algorithm
nfet	Gate NOT nwell
pfet	Gate AND nwell
nDiode	Ndiff AND DiodeID
Pdiff	diff AND nwell
pDiode	Pdiff AND DiodeID
diff_hole	Hole(diff)
diff_tap_nwell	tap_nwell INSIDE diff_hole
esd_diff_tap_nwell	ESDID AND diff_tap_nwell
Ndiff	diff NOT nwell
tap_nwell	tap INSIDE nwell
ESD_diffusion	A+B31ny diffusion or ESD_nwell_tap connected directly or through a resistor to a Pad or to Vss/Vcc t
ESD_cascode_diffusion	Diffusion covered by areaid.ed between two minimum spaced poly gates and located within a pair of d
ESD_diode	Any nwell (other than ESD_nwell_tap) covered by areaid.ed and areaid.de that does not contain poly
ESD_FET	(any Pdiff covered by areaid:ed within a double tap guardrings) OrnESD_NFET
ESD_NFET	(any Ndiff covered by areaid:ed abutting ESD_nwell_tap) Or (any Ndiff covered by areaid:ed abutting
I/O_or_Output_Pmos	ESD P+ diffusion overlapping poly and overlapping ESD source/drain diffusion connected to I/O or ou
I/O_Pmos_w/series_R	ESD PMOS connected to I/O or output net through series resistors
met_ESD_resistor	Metal resistor inside areaid:ed
Non_Vcc_nwell	Any nwell connected to any bias other than power supply
Nwell_area	Is determined using the following steps:n(a) Grow pdiff by 1.5 mmn(b) Mergen(c) And Nwell:dg
Pwell_area	Is determined using the following steps:n(a) Grow ndiff by 1.5 mmn(b) Mergen(c) NOT Nwell:dg
Series_transistors	Merged diffusion determined by Nwell_area and Pwell_area
fuse:dg	met2:fe for S8D*/S8TM*, met3.fe for S8TEE*/S8TNV/S8Q*/SP8TEE-5R/SP8Q*, met4.fe for S8P*/S
fuse_contact	(fuse_metal overlapping fuse:dg) NOT fuse:dg
fuse_metal	met3 for S8TEE*/S8TNV/S8Q*/SP8TEE-5R/SP8Q*; met2 for S8D*/S8TM*, met4 for S8P*/SP8P*
fuse_shield	Metal line (same metal level as fuse) between fuse and periphery, not overlapping contacts or vias, wit
non-isolated fuse edge	Long edge of the fuse spaced to Met2/Met3/Met4 less than a specified amount
single_fuses	Fuses without neighboring fuses within specified distance

5.4.2 Auxiliary Layers

Table 5.17: Table C4a: Purpose layer description in LSW window and Auxiliary Layers

waffle_chip	icfb ver 5.0	icfb ver 5.1
drawing	dg	drw
pin	pn	pin
boundary	by	bnd
net	nt	net
res	rs	res
label	ll	lbl
cut	ct	cut
short	st	sho
pin	pn	pin
gate	ge	gat
probe	pe	pro
blockage	be	blo
model	ml	mod
optionX (X = 1…n)	oX (X = 1..n)	opt*(X=1..n)
fuse	fe	fus
mask	mk	mas*
maskAdd	md	mas*
maskDrop	mp	mas*
waffleAdd1	w1	waffleAdd1
waffleAdd2	w2	waffleAdd2
waffleDrop	wp	waf
error	er	err
warning	wg	wng
dummy	dy	dmy

Table 5.18: Table C4b: Purpose layer description in LSW window and Auxiliary Layers

waffle_chip	icfb ver 5.0	icfb ver 5.1
drawing	dg	drw
pin	pn	pin
boundary	by	bnd
net	nt	net
res	rs	res
label	ll	lbl
cut	ct	cut
short	st	sho
pin	pn	pin
gate	ge	gat
probe	pe	pro
blockage	be	blo
model	ml	mod
optionX (X = 1…n)	oX (X = 1..n)	opt*(X=1..n)
fuse	fe	fus

Table 5.18 – continued from previous page

waffle_chip	icfb ver 5.0	icfb ver 5.1			
mask	mk	mas*			
maskAdd	md	mas*			
maskDrop	mp	mas*			
waffleAdd1	w1	waffleAdd1			
waffleAdd2	w2	waffleAdd2			
waffleDrop	wp	waf			
error	er	err			
warning	wg	wng			
dummy	dy	dmy			
Layout Data Name & GDSII No.	Brief description	icfb ver 5.1	Identifiesn(See WOLF-41, SPR 95111 for more details)	Who	Use
areaid.sl{81:1}	areaid sealring	areaid.sea	The area of the Seal ring	Tech	
areaid.ww{81:13	areaid Waffle Window	areaid.waf	Used to prevent waffle shifting. When larger than areaid:sl re-defines the placement of waffles.	Frame	CLDRC
areaid.dn{81:50}	areaid dead Zon	areaid.dea	"deadzone" area in the DieSealR pcell (Seal Ring) for metal stress relief rule checks	Tech	

Table 5.18 – continued from previous page

waffle_chip	icfb ver 5.0	icfb ver 5.1			
areaid.cr{81:51}	areaid crit-Corner	areaid.cri*	For portions of layout that are not to be put in the critical side do to stress constraints. Should be used sparingly and only over the portion of the layout to remove DRC violations. Avoid using a blanket polygon over the entire layout. This layer is to be used instead of using the noCritSideReg verification option in Stress.n"critical corner" area in the DieSealR pcell (Seal Ring) for metal stress relief rule checks	Tech	Stress
areaid.cd{81:52}	areaid critSid	areaid.cri*	"criticalsid" area in the DieSealR pcell (Seal Ring) for metal stress relief rule checks	Tech	Stress
areaid.ce{81:2}	areaid core	areaid.cor	Memory core (memory cells and approved on-pitch only)	Tech	DRC
areaid.fe{81:3}	areaid frame	areaid.fra*	Pads in the frame	Frame	DRC

Table 5.18 – continued from previous page

waffle_chip	icfb ver 5.0	icfb ver 5.1			
areaid.ed{81:19}	areaid ESD	areaid.esd	ESD devices- Surrounds any diffusion or ESD nwell tap connected to a signal pad. (only over ESD devices with special poly/tap exemption rules per LFL)	ESD, Des	DRC
areaid.dt{81:11}	areaid die cut	areaid.die	Location of the die within the frame used in frame builder ngeneration to create blanking for die and other drop-ins. Also used in cldrc/drc for rules in frame to die edge (waffles, nsm, metals etc)	Frame	Tech
areaid.mt{81:10}	areaid module cut	areaid.mod	Location of e-test modules within the frame used in frame builder gener- ation to create data in scribe lane(example: opaque/clear masks) and to mark location of cells (etest and fab)for frame reports. Also used in drc/cldrc for rules to cell edge.	Frame	Tech
areaid.ft{81:12}	areaid frameRect	areaid.fra*	Boundary of the frame used in frame builder generation to mark boundary of frame. Also used in cldrc/drc for rules to frame edge	Frame	DRC/CLDRC

Table 5.18 – continued from previous page

waffle_chip	icfb ver 5.0	icfb ver 5.1			
areaid.de{81:23}	areaid Diode	areaid.dio	The area occupied by diodes; Used to identify diodes during LVS	All	LVS
areaid.sc{81:4}	areaid standardc	areaid.sta	Cells in the standard cell library (over standard cell IP blocks only) .	Standard cell	DRC
areaid.st{81:53}	areaid SubstrateCut	areaid.sub	Regions to be considered as isolated substrates (only to designate 2 different resistively connected substrate nregions, >100um apart)	Tech, Des, ESD	Latch up, LVS, soft
areaid.en{81:57}	areaid extended drain	areaid.ext	Used to identify the extended drain devices	Tech, Des, ESD	LVS
areaid.le{81:60}	areaid LV Native	areaid.lvn	Used to identify the 3V Native NMOS versus 5V Native NMOS	Tech, Des	LVS
areaid.po{81:81}	areaid photo	areaid.pho	The areaid id is to identify the dnwell photo diode	Tech, Des	DRC
areaid.et{81:101	areaid etest	areaid.ete	Used in etest modules	Frame	DRC

Table 5.18 – continued from previous page

waffle_chip	icfb ver 5.0	icfb ver 5.1			
areaid.ld{81:14}	areaid low tap density	areaid.low	6um tap to diff rule will not be checked in this regionn-Diffusion >6u from related tap, requiring >50u from sigPadDiff && sigPadMet-Ntr).nShould be used sparingly and only over the portion of the layout to remove DRC violations. This layer is not to be used if a tapping solution can be found. This layer can only be used if there is low risk for latchup. This layer will be reviewed during PDQC.	All	DRC
areaid.ns{81:15}	areaid not-crtical side	areaid .not	critSideReg stress rules will not be checked in this regionnCannot be placed in the critical side – uncommon, or where stress nerrors can't be fixed)	All	DRC

Table 5.18 – continued from previous page

waffle_chip	icfb ver 5.0	icfb ver 5.1			
areaid.ij{81:17}	areaid injection	areaid.inj	Identify all circuits that are susceptible to injection and ensure no signal-pad connected diffusion is within 100u.n"areaid.inj' encloses any circuitry deemed sensitive (by design team) to injected substrate areaid.inj encloses any PVT compliant circuitry	All	DRC
areaid.hl{81:63}	areaid.hvnwell	areaid.hvn	Identify nwell hooked to HV but containing FETs with thin oxide; nPotential difference across the FET terminals is LVnUsed over lv devices, operating in lv mode, placed in hv nwells, and should NOT have hvi	All	DRC
areaid.re{81:125	areaid rf diode	areaid.rfd	Defines rf diodes that need to be extracted with series resistance (memo GCZ-124/125)	All	LVS
areaid.rd{81:24}	areaid.rdlprobepa	areaid.rdl	Ignore RDL keepouts when opening up PMM2	All	CLDRC

Table 5.18 – continued from previous page

waffle_chip	icfb ver 5.0	icfb ver 5.1			
areaid.sf{81:6}	areaid sigPad-Diff		Identify all srdrn diffusions and tap which are intended to be nconnected to signal pad (io Nets). Goes over diffusions connected to a signal pad - including through a poly resistor	All	LATCHUP
areaid.sl{81:7}	areaid.sigPadWell		Identify all nwells and pwells which are intended to be connected to signal pad (io Nets). Goes over wells with tap connected to a signal pad, including through a poly resistor	All	LATCHUP
areaid.sr{81:8}	areaid sigPad-MetNtr		Identify all srcdrn, tap, and wells which are intended to be nmetallically connected to signal pad (io Nets) not through a resistor. nMust be used in unison with areaid.sigPadDifff or areaid.sigPadWell with one of the above 2 areaids, nodes metallically nconnection to a sigPad (not through res)	All	LATCHUP
inductor:dg{82:24}	ID layer for inductor		Inductors	Tech, Des	DRC

continues on next page

Table 5.18 – continued from previous page

waffle_chip	icfb ver 5.0	icfb ver 5.1			
t1,2,3 {82:26, 27, 28}	terminal labels for inductor		Labels required by inductor terminals to be recognized as device	Tech, Des	LVS
poly:ml {66:83}	poly device model		Model name extraction	Tech, Des, ESD	LVS
ncm {92:44}	N-Core Implant		Ncm.dg is available as a drawn layer	All	DRC/CLDRC
protect)	VPP capacitor		Interdigitated, vertical Li1, M1 and M2 capacitor	All	LVS
capm_2t.dg	MIM caps (2 terminal model)		ID layer for MIMCAP that will be treated as 2T device	All	DRC/LVS
cpmm:dg{91}	Drawn compatible polyimide layer		Drawn compatible layer and used only inside S8 RF pad	Frame	
li1.be{67:10}	li1 blockage layer		Li1 blockage layer used for IP integration (per CWR 137)	All	DRC
met1.be{68:10}	Metal1 blockage layer		Metal 1 blockage layer used for IP integration (per CWR 137)	All	DRC
met2.be{69:10}	Metal2 blockage layer		Metal 2 blockage layer used for IP integration (per CWR 137)	All	DRC
met3.be{70:10}	Metal3 blockage layer		Metal 3 blockage layer used for IP integration (per CWR 137)	All	DRC
met4.be{71:10}	Metal4 blockage layer		Metal 4 blockage layer used for IP integration (per CWR 137)	All	DRC

Table 5.18 – continued from previous page

waffle_chip	icfb ver 5.0	icfb ver 5.1			
met5.be{72:10}	Metal5 blockage layer		Metal 5 blockage layer used for IP integration (per CWR 137)	All	DRC
vhvi {74:21}	Very High voltage id layer		Used to identify nodes that operate at 12V nominal (16V max)	Des	VHV Rules
uhvi {74:22}	Ultra High voltage id layer		Used to identify nodes that operate at 20V nominal	Des	UHV Rules
areaid.e0{81:58}	Area extended drain	areaid.ext	Used to identify 20V drain extended devices	Des	LVS
areaid.zr{81:18}	Area zener diode	areaid.zen	Used to identify Zener diodes	Des	LVS
fom.dy{}	FOM dummy		FOM waffle drawn in this layer	All	Waffles
prune:dg{84:44}	prune		Areas ignored by LVS	Frame	LVS
areaid:cr {81:55}	copper pillar (.cuPillar)	areaid.cup	Placement of Cu pillar over the pad area, streamed out to Amkor, s8pfhd-10r flow only	Die	CLDRC s8pfhd-10r
cyprotect.dg {56.44}	External F25 layer	cyprotect.dg	Switch to direct streaming to drawn (no protect) or mask layer (with protect)	Frame	CLDRC
cytextmc.dg {50:44}	Locations for mask compose	cytextmc.dg	Text to extract placement for Fab25 tool	Frame	CLDRC
cypsbr.dg {51:44}	No phaseshift allowed	cypsbr.dg	Phaseshift layer common to all F25 phaseshift masks	Frame	
areaid:ag{81:79}	analog	areaid.ana	Used to identify analog circuits	All	Analog
natfet.dg {124:21}	DEFETs	natfet.dg	Add TUNM for SONOS channel implants. See SPR 117559, SGL-529	All	DRC/CLDRC

Table 5.18 – continued from previous page

waffle_chip	icfb ver 5.0	icfb ver 5.1		
areaid:lw	Ultra High voltage id layer	Areaid low voltage: UHV box to put all HV/LV curcuits in	All	Analog
	• To distinguish the layers, the full name of the layer needs to be turned on in the LSW window			
	As the layers are displayed in LSW window in icfb version 5.0; For purpose layer displayed in version 5.1, pls refer table C3			

5.4.3 Devices and Layout vs Schematic (LVS) Information

Table 5.19: Table F2a: Devices and Layout vs. Schematic (LVS)

waffle_chip	icfb ver 5.0	icfb ver 5.1
drawing	dg	drw
pin	pn	pin
boundary	by	bnd
net	nt	net
res	rs	res
label	ll	lbl
cut	ct	cut
short	st	sho
pin	pn	pin
gate	ge	gat
probe	pe	pro
blockage	be	blo
model	ml	mod
optionX (X = 1…n)	oX (X = 1..n)	opt*(X=1..n)

Table 5.19 – continued from previous page

waffle_chip	icfb ver 5.0	icfb ver 5.1			
fuse	fe	fus			
mask	mk	mas*			
maskAdd	md	mas*			
maskDrop	mp	mas*			
waffleAdd1	w1	waffleAdd1			
waffleAdd2	w2	waffleAdd2			
waffleDrop	wp	waf			
error	er	err			
warning	wg	wng			
dummy	dy	dmy			
Layout Data Name & GDSII No.	Brief description	icfb ver 5.1	Identifiesn(See WOLF-41, SPR 95111 for more details)	Who	Use
areaid.sl{81:1}	areaid sealring	areaid.sea	The area of the Seal ring	Tech	
areaid.ww{81:13	areaid Waffle Window	areaid.waf	Used to prevent waffle shifting. When larger than areaid:sl re-defines the placement of waffles.	Frame	CLDRC
areaid.dn{81:50}	areaid dead Zon	areaid.dea	"deadzone" area in the DieSealR pcell (Seal Ring) for metal stress relief rule checks	Tech	

continues on next page

Table 5.19 – continued from previous page

waffle_chip	icfb ver 5.0	icfb ver 5.1			
areaid.cr{81:51}	areaid crit-Corner	areaid.cri*	For portions of layout that are not to be put in the critical side do to stress constraints. Should be used sparingly and only over the portion of the layout to remove DRC violations. Avoid using a blanket polygon over the entire layout. This layer is to be used instead of using the noCritSideReg verification option in Stress.n"critical corner" area in the DieSealR pcell (Seal Ring) for metal stress relief rule checks	Tech	Stress
areaid.cd{81:52}	areaid critSid	areaid.cri*	"criticalsid" area in the DieSealR pcell (Seal Ring) for metal stress relief rule checks	Tech	Stress
areaid.ce{81:2}	areaid core	areaid.cor	Memory core (memory cells and approved on-pitch only)	Tech	DRC
areaid.fe{81:3}	areaid frame	areaid.fra*	Pads in the frame	Frame	DRC

Table 5.19 – continued from previous page

waffle_chip	icfb ver 5.0	icfb ver 5.1			
areaid.ed{81:19}	areaid ESD	areaid.esd	ESD devices-Surrounds any diffusion or ESD nwell tap connected to a signal pad. (only over ESD devices with special poly/tap exemption rules per LFL)	ESD, Des	DRC
areaid.dt{81:11}	areaid die cut	areaid.die	Location of the die within the frame used in frame builder ngeneration to create blanking for die and other drop-ins. Also used in cldrc/drc for rules in frame to die edge (waffles, nsm, metals etc)	Frame	Tech
areaid.mt{81:10}	areaid module cut	areaid.mod	Location of e-test modules within the frame used in frame builder generation to create data in scribe lane(example: opaque/clear masks) and to mark location of cells (etest and fab)for frame reports. Also used in drc/cldrc for rules to cell edge.	Frame	Tech
areaid.ft{81:12}	areaid frameRect	areaid.fra*	Boundary of the frame used in frame builder generation to mark boundary of frame. Also used in cldrc/drc for rules to frame edge	Frame	DRC/CLDRC

Table 5.19 – continued from previous page

waffle_chip	icfb ver 5.0	icfb ver 5.1			
areaid.de{81:23}	areaid Diode	areaid.dio	The area occupied by diodes; Used to identify diodes during LVS	All	LVS
areaid.sc{81:4}	areaid standardc	areaid.sta	Cells in the standard cell library (over standard cell IP blocks only) .	Standard cell	DRC
areaid.st{81:53}	areaid SubstrateCut	areaid.sub	Regions to be considered as isolated substrates (only to designate 2 different resistively connected substrate nregions, >100um apart)	Tech, Des, ESD	Latch up, LVS, soft
areaid.en{81:57}	areaid extended drain	areaid.ext	Used to identify the extended drain devices	Tech, Des, ESD	LVS
areaid.le{81:60}	areaid LV Native	areaid.lvn	Used to identify the 3V Native NMOS versus 5V Native NMOS	Tech, Des	LVS
areaid.po{81:81}	areaid photo	areaid.pho	The areaid id is to identify the dnwell photo diode	Tech, Des	DRC
areaid.et{81:101	areaid etest	areaid.ete	Used in etest modules	Frame	DRC

Table 5.19 – continued from previous page

waffle_chip	icfb ver 5.0	icfb ver 5.1			
areaid.ld{81:14}	areaid low tap density	areaid.low	6um tap to diff rule will not be checked in this regionn-Diffusion >6u from related tap, requiring >50u from sigPadDiff && sigPadMet-Ntr).nShould be used sparingly and only over the portion of the layout to remove DRC violations. This layer is not to be used if a tapping solution can be found. This layer can only be used if there is low risk for latchup. This layer will be reviewed during PDQC.	All	DRC
areaid.ns{81:15}	areaid not-crtical side	areaid .not	critSideReg stress rules will not be checked in this regionnCannot be placed in the critical side – uncommon, or where stress nerrors can't be fixed)	All	DRC

Table 5.19 – continued from previous page

waffle_chip	icfb ver 5.0	icfb ver 5.1			
areaid.ij{81:17}	areaid injection	areaid.inj	Identify all circuits that are susceptible to injection and ensure no signal-pad connected diffusion is within 100u.n"areaid.inj' encloses any circuitry deemed sensitive (by design team) to injected substrate areaid.inj encloses any PVT compliant circuitry	All	DRC
areaid.hl{81:63}	areaid.hvnwell	areaid.hvn	Identify nwell hooked to HV but containing FETs with thin oxide; nPotential difference across the FET terminals is LVnUsed over lv devices, operating in lv mode, placed in hv nwells, and should NOT have hvi	All	DRC
areaid.re{81:125	areaid rf diode	areaid.rfd	Defines rf diodes that need to be extracted with series resistance (memo GCZ-124/125)	All	LVS
areaid.rd{81:24}	areaid.rdlprobepa	areaid.rdl	Ignore RDL keepouts when opening up PMM2	All	CLDRC

Table 5.19 – continued from previous page

waffle_chip	icfb ver 5.0	icfb ver 5.1			
areaid.sf{81:6}	areaid sigPad-Diff		Identify all srdrn diffusions and tap which are intended to be nconnected to signal pad (io Nets). Goes over diffusions connected to a signal pad - including through a poly resistor	All	LATCHUP
areaid.sl{81:7}	areaid.sigPadWell		Identify all nwells and pwells which are intended to be connected to signal pad (io Nets). Goes over wells with tap connected to a signal pad, including through a poly resistor	All	LATCHUP
areaid.sr{81:8}	areaid sigPad-MetNtr		Identify all srcdrn, tap, and wells which are intended to be nmetallically connected to signal pad (io Nets) not through a resistor. nMust be used in unison with areaid.sigPadDifff or areaid.sigPadWell with one of the above 2 areaids, nodes metallically nconnection to a sigPad (not through res)	All	LATCHUP
inductor:dg{82:24}	ID layer for inductor		Inductors	Tech, Des	DRC

Table 5.19 – continued from previous page

waffle_chip	icfb ver 5.0	icfb ver 5.1			
t1,2,3 {82:26, 27, 28}	terminal labels for inductor		Labels required by inductor terminals to be recognized as device	Tech, Des	LVS
poly:ml {66:83}	poly device model		Model name extraction	Tech, Des, ESD	LVS
ncm {92:44}	N-Core Implant		Ncm.dg is available as a drawn layer	All	DRC/CLDRC
protect)	VPP capacitor		Interdigitated, vertical Li1, M1 and M2 capacitor	All	LVS
capm_2t.dg	MIM caps (2 terminal model)		ID layer for MIMCAP that will be treated as 2T device	All	DRC/LVS
cpmm:dg{91}	Drawn compatible polyimide layer		Drawn compatible layer and used only inside S8 RF pad	Frame	
li1.be{67:10}	li1 blockage layer		Li1 blockage layer used for IP integration (per CWR 137)	All	DRC
met1.be{68:10}	Metal1 blockage layer		Metal 1 blockage layer used for IP integration (per CWR 137)	All	DRC
met2.be{69:10}	Metal2 blockage layer		Metal 2 blockage layer used for IP integration (per CWR 137)	All	DRC
met3.be{70:10}	Metal3 blockage layer		Metal 3 blockage layer used for IP integration (per CWR 137)	All	DRC
met4.be{71:10}	Metal4 blockage layer		Metal 4 blockage layer used for IP integration (per CWR 137)	All	DRC

Table 5.19 – continued from previous page

waffle_chip	icfb ver 5.0	icfb ver 5.1			
met5.be{72:10}	Metal5 blockage layer		Metal 5 blockage layer used for IP integration (per CWR 137)	All	DRC
vhvi {74:21}	Very High voltage id layer		Used to identify nodes that operate at 12V nominal (16V max)	Des	VHV Rules
uhvi {74:22}	Ultra High voltage id layer		Used to identify nodes that operate at 20V nominal	Des	UHV Rules
areaid.e0{81:58}	Area extended drain	areaid.ext	Used to identify 20V drain extended devices	Des	LVS
areaid.zr{81:18}	Area zener diode	areaid.zen	Used to identify Zener diodes	Des	LVS
fom.dy{}	FOM dummy		FOM waffle drawn in this layer	All	Waffles
prune:dg{84:44}	prune		Areas ignored by LVS	Frame	LVS
areaid:cr {81:55}	copper pillar (.cuPillar)	areaid.cup	Placement of Cu pillar over the pad area, streamed out to Amkor, s8pfhd-10r flow only	Die	CLDRC s8pfhd-10r
cyprotect.dg {56.44}	External F25 layer	cyprotect.dg	Switch to direct streaming to drawn (no protect) or mask layer (with protect)	Frame	CLDRC
cytextmc.dg {50:44}	Locations for mask compose	cytextmc.dg	Text to extract placement for Fab25 tool	Frame	CLDRC
cypsbr.dg {51:44}	No phaseshift allowed	cypsbr.dg	Phaseshift layer common to all F25 phaseshift masks	Frame	
areaid:ag{81:79}	analog	areaid.ana	Used to identify analog circuits	All	Analog
natfet.dg {124:21}	DEFETs	natfet.dg	Add TUNM for SONOS channel implants. See SPR 117559, SGL-529	All	DRC/CLDRC

<div align="center">Table 5.19 – continued from previous page</div>

waffle_chip	icfb ver 5.0	icfb ver 5.1			
areaid:lw	Ultra High voltage id layer		Areaid low voltage: UHV box to put all HV/LV curcuits in	All	Analog
	• To distinguish the layers, the full name of the layer needs to be turned on in the LSW window				
	As the layers are displayed in LSW window in icfb version 5.0; For purpose layer displayed in version 5.1, pls refer table C3				

Explanation of symbols:

- – = Layer illegal for the device

- + = Layer allowed to overlap

- D = DRAWN indicates that a layer is drawn by Design.

- C = CREATED indicates that the layer is only created by CAD.

Table 5.20: Table F2b: Mask Generation table

Category	Name	Used	Layout Mask required element	FO	D	P'	P'	N	H'	LV	N	TL	O	LV	R	P	H'	N'	LIN'	N	N	P	LI	LI	C	M	M	M	M	C	IN	Drawn Route / Comments
R SI TC	n di re sis to	re r	sk	C																C											
R SI TC	H n di re sis to	re r	m	C					C			C	C				C														
R SI TC	p di re sis to	re r	sk	C			C	C		C							C			C											
R SI TC	p di re sis to N	re r	sk	C			C	C		C							C			C											
R SI TC	H p di re sis to	re r	m	C			C			C			C				C														
R SI TC	Iso lat Pv re sis to	re sp	sk	C	C																										
R SI TC	n+ po re sis to	re	sk									C																				

continues on next page

Table 5.20 – continued from previous page

C e- g	N	U	La ou M ar re qu sc el e- m	F	D	P D	P	N	H	L	N	T	O	L	R	P	H	N N	LI	N	N	P	LI	LI	C	M	M	M	M	C	IN	Drawn Route / Com- ments
R Sl T(	p+ po re si: to	re	xl							C	C		C		C		C															
R Sl T(	li re si: to	re	sk																C													
R Sl T(	m fu	m	m																							C				metX AND metX.fe
R Sl T(	m fu	m	m																							C				metX AND metX.fe
3: A C	nr 1.	nf	sk	C										C					C											
3: A C	pr 1.	pf	sk	C				C	C		C				C	C			C											
3: A C N	pr 1.	pf	sk	C				C	C		C				C	C			C											
3: A C	Lc V pr 1. 3:	pf	sk	C				C		C					C	C			C											
3: A C	H: V pr 1. 3:	pf	sk	C				C	C	C	C				C	C			C											

Table 5.20 – continued from previous page

Cetego	N;	U;	LaouMarrequscelem	F(	D	P'	P'D	N'	H'	L\	N	Tl	O	L\	R	P'	H'	N'N'	LI	N	N;	P;	LI	LI	C	M	M	M	M	C	IN	Drawn Route / Comments
3; A C 1. 3; N	H; V; pr	pf	sk	C				C	C	C	C					C		C				C										
3; A C 1. 3;	L(V; nr	nf	sk	C					C							C			C													
3; A C	nr	nf	sk	C												C			C													
3; A C	nr	nf	sk	C												C			C													
3; A C	nr N	nf	sk	C						C						C		C	C													
3; A C	nr N	nf	sk	C					C							C		C	C													
3; A C	pr	pf	sk	C				C	C	C	C					C		C				C										
3; A C	pr N	pf	sk	C				C	C	C						C		C				C										
3; A C	L(V; nr			C					C							C			C													

continues on next page

Table 5.20 – continued from previous page

Cate-gory	Na	U:	La ou M ar re qu sc el e-m	F(	D	P'	P'D	N'	H'	L\	N	T(	O	L\	R	P'	H'	N'N	N:	N:	P:	LI	LI	C:	M	M	M	M	C:	IN	Drawn Route / Com-ments
32 A C	L(V: V: ac to	ca	sk	C			C	C							C	C		C													
32 A C	H: V: V: ac to	ca	sk	C		C	C	C	C						C	C		C													
32 A C	H va ac to (fl in ga			C	C		C	C			C		C	C	C		C													
S((8 S(L:	S(fe	nf	sk	C	C		C		C	C	C		C		C	C		C													
S((8 S(L:	S(fe	nf	sk	C	C		C		C	C	C		C		C	C		C													
S((8 S(L:	N' S(fe	nf S(	nv so	C			C		C	C	C		C		C	C		C													
S((8 S(L:	N' S(fe	nf S(	nv so	C			C		C	C	C		C		C	C		C													
1' C	H nr 5/	nf	sk	C						C		C	C	C		C															
1' C	H pr 5/ V	pf	sk	C			C			C		C	C			C			C												

continues on next page

Table 5.20 – continued from previous page

C e- g	N	U	L ou M ar re qu sc el e-m	F	D	P	P D	N	H	L	N	T	O	L	R	P	H	N	LI N	N	N	P	LI	LI	C	M	M	M	M	C	IN	Drawn Route / Com- ments
1 C	N tiv nr 5V	nf	sk	C				C		C				C	C	C		C														
1 C	N tiv nr 3V	nf	sk	C				C		C				C	C	C		C														
1 C	Fl np	nf	sk	C						C				C		C	C		C													
1 C	Fl np N	nf	nv rn pa	C						C				C		C	C		C													
1 C	V nr 5/ D	nf	sk	C			C			C				C	C	C		C														
1 C	V pr 5/ D	pf	sk	C	C		C			C				C		C							C									
1 C	U nr 5/ D	nf		C	C	C		C		C				C		C			C													
1 C	U iso nr 5/ D	nf		C	C	C		C		C				C		C			C													
1 C	U N tiv nr 5/ D	Tl		C	C	C		C		C				C		C			C													

continues on next page

Table 5.20 – continued from previous page

C e- g	N	U	La ou M ar re qu sc el e- m	F(	D	P' D	P'	N'	H'	L\	N	Tl	O	L\	R	P	H'	N' LI N	N	N	P	LI	LI	C	M	M	M	M	C	IN	Drawn Route / Com- ments
1 C	U N tiv is nr 5/ D	nf		C	C	C		C		C			C	C				C													
1 C	U pr 5/ D	pf		C	C	C	C	C		C			C	C				C													
C P/ l- T(	M	cr sk																					C		C						
C P/ l- T(	V	ca sk																				C		C	C						
C P/ l- T(	V (w m sh	vp pc																				C		C	C	C					
IN D T(	In du to	in du	sk																												C
IN D T(	C In du du to	in du	sk																										C	C	
IN D T(	B In du du to	in du	sk																										C	C	
D	nl	lv	sk	C										C																		

Table 5.20 – continued from previous page

Ce-go	N	U	La ou M ar re qu sc el e-m	F	D	P	P D	N	H	L	N	T	O	L	R	P	H	N N	LI	N	N	P	LI	LI	C	M	M	M	M	C	IN	Drawn Route / Com-ments
D	H nI	lv	sk	C						C				C	C			C														
D	Rl ES H nI	lv	sk	C						C				C	C			C														
D	Rl ES D N nI	lv		C	C					C				C	C			C														
D	pI	lv	sk	C			C	C		C					C			C														
D	pI N	lv	sk	C			C	C		C					C			C														
D	H pI	lv	sk	C			C				C				C			C														
D	Rl ES H pI	lv	sk	C			C				C				C			C														
D	Pl D	lv	dr	C	C		C	C		C					C			C														
D	L V pc	di	sk	C			C		C						C			C														
D	H V pI	di	sk	C			C	C	C	C					C			C														

Table 5.20 – continued from previous page

Category	Na	Us	Layout Mar req sc el em	F	D	P	P D	N	H	L\	N	Tl	O	L\	R	P	H	N	LI N	N	P	LI	LI	C	M	M	M	M	C	IN	Drawn Route / Comments
D	H V pI N	di	sk	C			C	C	C	C							C				C										
D	L V nI	di	sk	C				C									C														
D	N S(D	di	nc	C				C		C	C	C				C															
D	N tiv nI	di	sk	C				C			C			C	C																
D	N D	di	sk			C																										
D	Rl N D	di	sk			C																										
D	Pv D N D	di	sk		C																											
D	Rl E Pv D N D	di	sk		C																											
D	Rl Pv D N D	di	sk		C																											

Table 5.20 – continued from previous page

C e-go	N a	U s	L a ou M ar re qu sc el e-m	F(	D	P'	P'(D)	N'	H'	L'	N'	T(	O	L'	R	P'	H'	N'N'	L(	N(	N	P(	L(	L(	C,	M	M	M	C(	I(	Drawn Route / Comments
D	Ps D(N' D:	di	sk	C																											
D	Ps D(N' D:	di	sk	C	C																										
D	H' P\ D(N' D:	di	dr	C																											
Pl	Pa-sit Pl	pr	sk	C			C	C		C							C		C	C											Lay-out pro-vided by tech-nol-ogy
Pl	Pa-sit N.	pr	sk	C	C		C												C	C											Lay-out pro-vided by tech-nol-ogy
E! tra si: to	L\ nl tra si: to	nf	sk	C							C					C															NMOS with ESD_nwell_tap
E! tra si: to	H nl tra si: to	nf	sk	C					C		C	C	C				C													NMOS with ESD_nwell_tap

Table 5.20 – continued from previous page

C e-g	N U ou M ar re qu sc el e-m	L F D P P N H L N T O L R P H N L N N P L L C M M M M C I D N	Drawn Route / Com-ments
E tra si to	H N tiv nl tra si to	C C C C C C	
E tra si to	H pl tra si to	pf sk C C C C C C	

Explanation of symbols:

- `–` = Layer not created for the device
- `+` = Layer allowed to overlap
- `C` = CREATED
- `nr` = next revision

5.4.4 GDS Layers Information

The `gds_layers.csv file` provides a raw list of the layers used in the process with name, description and the GDS layer and data type.

Table 5.21: Table - GDS Layers

Layer name	Purpose	GDS layer:dat	Description
diff	drawing, text	65:20	Active (diffusion) area (type opposite of well/substrate underneath)
tap	drawing	65:44	Active (diffusion) area (type equal to the well/substrate underneath) (i.e., N+ and P+)
nwell	drawing	64:20	N-well region
dnwell	drawing	64:18	Deep n-well region
pwbm	drawing	19:44	Regions (in UHVI) blocked from p-well implant (DE MOS devices only)
pwde	drawing	124:20	Regions to receive p-well drain-extended implants
hvtr	drawing	18:20	High-Vt RF transistor implant

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[21] For RCX information

Table 5.21 – continued from previous page

Layer name	Purpose	GDS layer:data	Description
hvtp	drawing	78:44	High-Vt LVPMOS implant
ldntm	drawing	11:44	N-tip implant on SONOS devices
hvi	drawing	75:20	High voltage (5.0V) thick oxide gate regions
tunm	drawing	80:20	SONOS device tunnel implant
lvtn	drawing	125:44	Low-Vt NMOS device
poly	drawing, text	66:20	Polysilicon
hvntm	drawing	125:20	High voltage N-tip implant
nsdm	drawing	93:44	N+ source/drain implant
psdm	drawing	94:20	P+ source/drain implant
rpm	drawing	86:20	300 ohms/square polysilicon resistor implant
urpm	drawing	79:20	2000 ohms/square polysilicon resistor implant
npc	drawing	95:20	Nitride poly cut (under licon1 areas)
licon1	drawing	66:44	Contact to local interconnect
li1	drawing, text	67:20	Local interconnect
mcon	drawing	67:44	Contact from local interconnect to metal1
met1	drawing, text	68:20	Metal 1
via	drawing	68:44	Contact from metal 1 to metal 2
met2	drawing, text	69:20	Metal 2
via2	drawing	69:44	Contact from metal 2 to metal 3
met3	drawing, text	70:20	Metal 3
via3	drawing	70:44	Contact from metal 3 to metal 4
met4	drawing, text	71:20	Metal 4
via4	drawing	71:44	Contact from metal 4 to metal 5
met5	drawing, text	72:20	Metal 5
pad	drawing, text	76:20	Passivation cut (opening over pads)
nsm	drawing	61:20	Nitride seal mask
capm	drawing	89:44	MiM capacitor plate over metal 3
cap2m	drawing	97:44	MiM capacitor plate over metal 4
vhvi	drawing	74:21	12V nominal (16V max) node identifier
uhvi	drawing	74:22	20V nominal node identifier
npn	drawing	82:20	Base region identifier for NPN devices
inductor	drawing	82:24	Identifier for inductor regions
capacitor	drawing	82:64	Identifier for interdigitated (vertical parallel plate (vpp)) capacitors
pnp	drawing	82:44	Base nwell region identifier for PNP devices
LVS prune	drawing	84:44	Exemption from LVS check (used in e-test modules only)
ncm	drawing	92:44	N-core implant
padCenter	drawing	81:20	Pad center marker
target	drawing	76:44	Metal fuse target
areaid.sl	identifier	81:1	Seal ring identifier
areaid.ce	identifier	81:2	Memory (SRAM) core cell identifier
areaid.fe	identifier	81:3	Pads in padframe identifier
areaid.se	identifier	81:4	Standard cell identifier
areaid.st	identifier	81:6	Signal pad diffusion identifier (for latchup DRC checks)
areaid.sl	identifier	81:7	Signal pad well identifier (for latchup DRC checks)

Table 5.21 – continued from previous page

Layer name	Purpose	GDS layer:dat	Description
areaid.s	identifier	81:8	Signal pad metal (for latchup DRC checks)
areaid.m	identifier	81:10	Location of e-test modules within the frame
areaid.d	identifier	81:11	Location of dice within the frame
areaid.ft	identifier	81:12	Boundary of the frame
areaid.w	identifier	81:13	Waffle window (used to prevent waffle shifting)
areaid.lc	identifier	81:14	Low tap density (15um between taps) area. Must be at least 50um from pad-frame
areaid.n	identifier	81:15	Non-critical side. Blocks stress DRC rules
areaid.ij	identifier	81:17	Identification for areas susceptible to injection
areaid.z	identifier	81:18	Zener diode identifier
areaid.e	identifier	81:19	ESD device identifier
areaid.d	identifier	81:23	Diode identifier
areaid.r	identifier	81:24	RDL probe pad (not used in this process)
areaid.d	identifier	81:50	Dead zone (used in seal ring only for stress DRC)
areaid.c	identifier	81:51	Critical corner (used in seal ring only for stress DRC)
areaid.c	identifier	81:52	Critical side (used in seal ring only for stress DRC)
areaid.s	identifier	81:53	Substrate cut. Idendifies areas to be considered as isolated substrate
areaid.o	identifier	81:54	OPC drop. Block automatic OPC (for fab blocks and lithocal structures)
areaid.e	identifier	81:57	Extended drain identifier
areaid.e	identifier	81:58	20V Extended drain identifier
areaid.le	identifier	81:60	3.3V native NMOS identifier (absence indicates a 5V native NMOS)
areaid.h	identifier	81:63	HV nwell. Identifies nwells with thin oxide devices connected to high voltage
areaid.s	identifier	81:70	subcircuit identifier (for LVS extraction)
areaid.p	identifier	81:81	Photodiode device identifier
areaid.it	identifier	81:84	IP exempt from DFM rules
areaid.e	identifier	81:101	e-test module identifier
areaid.lv	identifier	81:108	Low-Vt identifier
areaid.re	identifier	81:125	RF diode identifier
fom	dummy	22:23	
poly	gate	66:9	
poly	model	66:83	(Text type)
poly	resistor	66:13	
diff	resistor	65:13	
pwell	resistor	64:13	
li1	resistor	67:13	
diff	high voltage	65:8	
met4	fuse	71:17	
inductor	terminal1	82:26	
inductor	terminal2	82:27	

Table 5.21 – continued from previous page

Layer name	Purpose	GDS layer:dat	Description
induc-tor	terminal3	82:28	
li1	block	67:10	
met1	block	68:10	
met2	block	69:10	
met3	block	70:10	
met4	block	71:10	
met5	block	72:10	
prB-ndry	boundary	235:4	
diff	boundary	65:4	
tap	boundary	65:60	
mcon	boundary	67:60	
poly	boundary	66:4	
via	boundary	68:60	
via2	boundary	69:60	
via3	boundary	70:60	
via4	boundary	71:60	
li1	label	67:5	(Text type)
met1	label	68:5	(Text type)
met2	label	69:5	(Text type)
met3	label	70:5	(Text type)
met4	label	71:5	(Text type)
met5	label	72:5	(Text type)
poly	label	66:5	(Text type)
diff	label	65:6	(Text type)
pwell	label	64:59	(Text and data type)
pwelliso	label	44:5	(Text type)
pad	label	76:5	(Text type)
tap	label	65:5	
nwell	label	64:5	
induc-tor	label	82:25	
text	label	83:44	(Text type)
li1	net	67:23	(Text type)
met1	net	68:23	(Text type)
met2	net	69:23	(Text type)
met3	net	70:23	(Text type)
met4	net	71:23	(Text type)
met5	net	72:23	(Text type)
poly	net	66:23	(Text type)
diff	net	65:23	(Text type)
li1	pin	67:16	(Text and data)

Table 5.21 – continued from previous page

Layer name	Purpose	GDS layer:data	Description
met1	pin	68:16	(Text and data)
met2	pin	69:16	(Text and data)
met3	pin	70:16	(Text and data)
met4	pin	71:16	(Text and data)
met5	pin	72:16	(Text and data)
poly	pin	66:16	(Text and data)
diff	pin	65:16	(Text and data)
nwell	pin	64:16	(Text type)
pad	pin	76:16	(Text and data)
pwell	pin	122:16	(Text and data)
pwelliso	pin	44:16	(Text and data)
nwell	pin	64:0	(Text type)
poly	pin	66:0	(Text type)
li1	pin	67:0	(Text type)
met1	pin	68:0	(Text type)
met2	pin	69:0	(Text type)
met3	pin	70:0	(Text type)
met4	pin	71:0	(Text type)
met5	pin	72:0	(Text type)
pad	pin	76:0	(Text type)
pwell	pin	122:0	(Text type)
diff	cut	65:14	
poly	cut	66:14	
li1	cut	67:14	
met1	cut	68:14	
met2	cut	69:14	
met3	cut	70:14	
met4	cut	71:14	
met5	cut	72:14	
pwell	cut		
met5	probe	72:25	
met4	probe	71:25	
met3	probe	70:25	
met2	probe	69:25	
met1	probe	68:25	
li1	probe	67:25	
poly	probe	66:25	
poly	short	66:15	
li1	short	67:15	
met1	short	68:15	
met2	short	69:15	
met3	short	70:15	
met4	short	71:15	
met5	short	72:15	

Table 5.21 – continued from previous page

Layer name	Purpose	GDS layer:dat	Description
Mask level data			
cncm	mask	17:0	N-core implant mask
crpm	mask	96:0	Resistor Protect mask
cpdm	mask	37:0	Pad mask
cnsm	mask	22:0	Nitride seal mask
cmm5	mask	59:0	Metal 5 mask
cviam4	mask	58:0	Via 4 mask
cmm4	mask	51:0	Metal 4 mask
cviam3	mask	50:0	Via 3 mask
cmm3	mask	34:0	Metal 3 mask
cviam2	mask	44:0	Via 2 mask
cmm2	mask	41:0	Metal 2 mask
cviam	mask	40:0	Via mask
cmm1	mask	36:0	Metal 1 mask
ctm1	mask	35:0	Contact mask
cli1m	mask	56:0	Local interconnect mask
clicm1	mask	43:0	Local interconnect contact mask
cpsdm	mask	32:0	P+ Implant mask
cnsdm	mask	30:0	N+ Implant mask
cldntm	mask	11:0	Lightly-doped N-tip implant mask
cnpc	mask	49:0	Nitride poly cut mask
chvntm	mask	39:0	High voltage N-tip implant mask
cntm	mask	27:0	N-tip implant mask
cp1m	mask	28:0	Poly 1 mask
clvom	mask	46:0	Low Voltage oxide mask
conom	mask	88:0	ONO Mask
ctunm	mask	20:0	Tunnel mask
chvtrm	mask	98:0	HLow VT PCh Radio mask
chvtpm	mask	97:0	High Vt Pch mask
clvtnm	mask	25:0	Low Vt Nch mask
cnwm	mask	21:0	Nwell mask
cdnm	mask	48:0	Deep nwell mask
cfom	mask	23:0	Field oxide mask
cfom	drawing	22:20	
clvtnm	drawing	25:44	
chvtpm	drawing	88:44	
conom	drawing	87:44	
clvom	drawing	45:20	
cntm	drawing	26:20	
chvntm	drawing	38:20	
cnpc	drawing	44:20	
cnsdm	drawing	29:20	
cpsdm	drawing	31:20	
cli1m	drawing	115:44	
cviam3	drawing	112:20	

Table 5.21 – continued from previous page

Layer name	Purpose	GDS layer:data	Description
cviam4	drawing	117:20	
cncm	drawing	96:44	
cntm	mask add	26:21	
clvtnm	mask add	25:43	
chvtpm	mask add	97:43	
cli1m	mask add	115:43	
clicm1	mask add	106:43	
cpsdm	mask add	31:21	
cnsdm	mask add	29:21	
cp1m	mask add	33:43	
cfom	mask add	22:21	
cntm	mask drop	26:22	
clvtnm	mask drop	25:42	
chvtpm	mask drop	97:42	
cli1m	mask drop	115:42	
clicm1	mask drop	106:42	
cpsdm	mask drop	31:22	
cnsdm	mask drop	29:22	
cp1m	mask drop	33:42	
cfom	mask drop	22:22	
cmm4	waffle drop	112:4	
cmm3	waffle drop	107:24	
cmm2	waffle drop	105:52	
cmm1	waffle drop	62:24	
cp1m	waffle drop	33:24	
cfom	waffle drop	22:24	
cmm5	waffle drop	117:4	

5.5 Device and Layout vs. Schematic

Table 5.22: Table F2a: Devices and Layout vs. Schematic (LVS)

Table 5.22 – continued from previous page

C e g	N	U	R q s e e m	d	d	d	c	t	d	p p d	p	h	n	h	l	p	p	n	t	h	r	p	p	p	p	l n	n	n	p c	li	li	li	li	c	c	m	m	m	m	m	m	m	r	i d t
RST	H n d re si tc	X	re re	D	D	D															D				D																				
RST	p d re si tc	X	re re	D	D	D			D							C										D																		
RST	p d re si tc N		re re	D	D	D			D							C										D																		
RST	H p d re si tc	X	re re sp	D	D	D			D									D								D																	
RST	Is la P re si tc	X	re sp			D	D						D	D																													
RST	n p re si tc	X	re																			D	D	D																		
RST	p p re si tc	X	re																			D	D	D	D		D	D														
RST	li re si tc	X	re																										D	D	D											

Table 5.22 – continued from previous page

Ceg	N	Uqseem	Rd	d	d	c	ta	d	p	p	h	n	h	lv	p	p	n	tu	h	rp	p	p	p	p	lcn	n	n	p	li-c	li	li	li	c	c	m	m	m	m	m	m	m	rc	ird to
FST	m	X	m																										D	D													
3AC	n1	X	n	D												D							D																				
3AC	p1	X	p	D					D	C				C		D							D																				
3AC Vp 13	L	X	p	D					D		D					D							D																				
3AC Vp 13	H	X	p	D					D	D	C					D							D																				
3AC Vn 13	L	X	n	D						D						D					D																						
3AC	n	X	n	D												D	D		D																								
3AC N	n		n	D										D		D	D	D		D																							
3AC	p	X	p	D					D	D	C			D		D		D			D																						
3AC N	p		p	D					D	D	C			D		D		D			D																						

Table 5.22 – continued from previous page

C e g	N	U	R q s e e m	d	d	d	c	t a	d	p	p d	h	n	h	l v	p	p	n	t u	h	r p	p	p	p	p	l c n	n	n	p	l i c	li	li	li	c	c	m	m	m	m	m	m	m	r c	i r d t
3 A C n	L V	X	n	D							D					D		D		D																									
3 A C V a t	L V	X	c			D				D	C					D				D																								
3 A C V a t	H V	X	c			D			D	D	C		C			D				D																								
3 A C v a t (f i g	H	X	c			D				D	D			D		D				D																								
S (8 S L	S f	X	n	D			D				D			D		D			D	D																								
S (8 S L	S f		n	D			D				D			D		D			D	D																								
S (8 S L	N S f		n	D							D			D		D		D	D	D																								
1 C n 5	H n	X	n	D											D		D				D																							
1 C n 5	H n		n	D											D		D		D		D																							
1 C p 5	H p	X	p	D						D					D		D									D																		

Table 5.22 – continued from previous page

C e g	N	U	R q s e e m	d	d	d	c	t a	d	p	p d	h	n	h	l v	p	p	n	t	h	r p	p	p n	p	p	l c	n	n	p	l i c	l i	l i	l i	c	c	m	m	m	m	m	m	r c	i r d t
1 C	H p 5		p	D								D					D	D				D																						
1 C	N ti n 5	X	n	D							D					D	D					D																					
1 C	N ti n 3	X	n	D							D					D	D					D																					
1 C	F n	X	n	D												D	D		D	D		D																					
1 C	F n N		n	D												D	D		D	D		D																					
1 C	V n 5 D	X	n te	D		D				D						D	D					D																					
1 C	V p 5 D	X	p te	D		D	D		D							D	D						D																				
1 C	U n 5 D		n te	D		D	D	D	D	D						D	D					D																					
1 C	U is n 5 D		n te	D		D	D	D	D	D						D	D					D																					
1 C	U N ti n 5 D		n te	D		D	D	D	D	D						D	D					D																					

Table 5.22 – continued from previous page

Ceg	N	U	Rqseem	d	d	d	c	ta	d	p	pd	h	n	h	lv	p	p	n	tu	h	rp	p	p	p	p	ln	n	n	p	lic	li	li	li	li	c	c	m	m	m	m	m	m	m	rc	ird tc
1C	UZn5,D	n te	D			D	D	D		D		D						D		D						D																			
1C	Up5,D	p te	D			D	D	D	D		D		D						D		D						D																		
CPl-T	M (3 T m n	c																														D			D										
CPl-T	M (2 T m n	c																													D	D			D										
CPl-T	V	X																													D			D	D										
CPl-TNNT	Vo N	X	ca																											D			D	D										
CPl-T	Vo P	X	ca																											D			D	D										
CPl-TNNT	V a N	X	vp pca																											D			D	D	D									
CPl-T	4 T V (v M sl	X	vp pca																											D			D	D	D									

Table 5.22 – continued from previous page

C e g	N	U	R q s e e m	d	d	d	c	t	d d	p	p	h	n	h	l v	p	p	n	t	h	r p	p	p	p	p	l n	n	n	p	l i c	l i	l i	l i	c	c	m	m	m	m	m	m	m	r	i r d t
C P l- T	4 te V (v N sl	X	v p c																							D						D	D	D	D	D									
C P l- T	4 te V (v N sl	X	v p c																							D						D	D	D	D										
C P l- T	3 T V	X	c																							D						D	D											
C P l- T	3 T V (f S C	X	c																							D						D	D	D										
C P l- T	3 T V (f S C	X	c																							D						D	D	D	D										
I D T	Ir d tc		ir d tc																																		D							D
I D T	C Ir d tc	X	ir																																D		D	D	D	D	D
I D T	B Ir d tc	X																																				D	D	D	D

Table 5.22 – continued from previous page

C e g	N	U	R q s e e m	d	d	d	c	t a	d	p	p d	h	n	h	l v	p	p	n	t	h	r	p n	p	p	p	p	l c	n	n	p c	li	li	li	li	c	c	m	m	m	m	m	m	m	m	r	ir d t
D	n	X	lv d	D																							D																			
D	H n	X	lv d	D									n								D						D																		
D	R E H n	X	lv d	D									n								D						D																		
D	R E H D N n	X	lv d	D				D					n								D						D																		
D	p	X	lv d	D						D							C										D																		
D	p N		lv d	D						D							C										D																		
D	H p	X	lv d	D						D									D								D																		
D	R E H p	X	lv d	D						D									D								D																		
D	P D	X	lv d				D	D		D																	D																		
D	L V p	X	d	D						D	D																D																		

Table 5.22 – continued from previous page

C e g	N	U	R q s e e m	d	d	d	c	ta	d	p d	p	h	n	h	lv	p	p	n	tu	h	rp	p	p	p	p	lc n	n	n	p c	li-	li	li	li	c	c	m	m	m	m	m	m	m	r	ir d t
D	H V p	X	d	D								D	D	C																D															
D	H V p N		d	D								D	D	C		C														D															
D	L V n	X	d	D									D													D																		
D	N S D		d	D									D			D					D																							
D	N ti n	X	d	D									D				D																											
D	N D	X	d								D																																	
D	N	X	lv d								D																																	
D	N	X	lv d								D																																	
D	R N D	X	d								D																																	
D	P D N D	X	d					D																																				

Table 5.22 – continued from previous page

C e g	N	U	R q s e e m	d	d	d	c	ta	d	p	p d	h	n	h	lv	p	p	n	tı	h	rı	p	p	p	p	lc n	n	n c	p	li-	li	li	li	c	c	m	m	m	m	m	m	m	rc	ir d tc
D	R E P D N D	X	lv dı						D																																			
D	R P D N D	X	dı						D																																		
D	P D N D	X	dı						D																																		
D	P D N D	X	lv dı						D																																		
D	P D N D	X	lv dı						D																																		
D	P D N D		dı						D	D																																		
D	H P D N D		dı						D		D																																
P	P a- si P	X	pı	D				D			D																							D	D								

Table 5.22 – continued from previous page

Ceg	N	U	Rqseem	d	d	d	c	ta	d	pd	p	h	n	h	lv	p	p	n	tu	h	rp	p	p	p	p	lcn	n	n	plc	li-	li	li	li	c	c	m	m	m	m	m	m	m	m	rc	irdtc
P PasiHGN	P	X	np	D			D			D								D		D						D	D																		
P PasiN	P	X	np	D			D			D																D	D																	
Etrsitc	Lntrsitc	X	n	D														D								D																		
Etrsitc	Hntrsitc	X	n	D											D		D								D																		
Etrsitc	HNtinitrsitc	X	n	D						D					D		D								D																		
Etrsitc	Hptrsitc	X	p	D						D					D		D								D																		

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[2] Ncm is drawn inside core. Otherwise it is created in periphery. See rules ncm.X.* for details

[20] mrp1 can't overlay capacitor.dg: exempted s8rf2_xcmvpp11p5x11p7_lim5shield from the rule

[10] LVS will check that phighvt inside areaid.ce overlaps ncm

[5] The 2 core FETs and flash npass must have a poly.ml label with their model name.

[11] The default model is sonos_e, sonos_de and nvssonos_e. If sonos_p, sonos_dp and nvssonos_p model are required, poly.ml must be used

[3] Drawn over half of device

[7] over the source

[6] over the drain

[9] Uses a black box for LVS. This is a fixed layout; Use symbol provided by modeling group

[12] The capacitor.dg is drawn 0.17um from the edge of the cell to be LVS clean

[16] There are multiple configurations of the Cu inductor. The layers present in one configuration may not be drawn in the other configuration. Also rdl will not be routed over met5 cu inductor, not checkable by CAD flow.

[15] Tech element is created by the user, no CAD supplied tech element

[13] Devices are LVS'ed by cell name, m=1 per cell, fixed area and perimeter (see QHC-18)

[8] Information for RCX

[17] Used for substrate noise isolation regions only

[19] Psub-Deep Nwell Diode must have condiode text "condiodeHvPsub"; CVA-596

[18] Either UHVI or areaid.low_vt should be drawn over the sturctures

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5.5. Device and Layout vs. Schematic

5.6 Summary of Key Periphery Rules

Table 5.23: Table F3a: Front end layers (Low Voltage Devices)

Layer	CD	nwell		diff		tap		n/psd		poly		npc		li-con	Manual
Parameter	width	spc	enc	spc	enc	spc	enc	spc	enc	spc	enc	spc	enc	spc	merg?
nwell	0.840	1.270	X	X	X	X	X	X	X	X	X	X	X	X	Yes
diff	0.150	0.340	0.180	0.270	X	X	X	X	X	X	X	X	X	X	•
tap	0.150	0.130	0.180	0.270	•	0.270	X	X	X	X	X	X	X	X	•
n/psd	0.380	•	•	0.130	0.130	0.130	0.130	0.380	X	X	X	X	X	X	Yes
poly on diff	0.150	•	•	•	•	0.300	•	•	•	0.210	X	X	X	X	•
poly on field	0.150	•	•	0.075	•	0.055	•	•	•	0.210	X	X	X	X	•
npc	0.270	•	•	•	•	•	•	•	•	0.090	X	0.270	X	X	Yes
li-con	0.170	•	•	•	0.04/0.06	•	0.000	•	•	0.055	•	0.090	•	0.170	•
poly_	0.170	•	•	0.190	illegal	0.190	illegal	•	•	0.080	•	0.100	•	0.170	•

Table 5.24: Table F3b: Front end layers (High Voltage Devices)

Layer	CD	nwell		diff		tap		poly		lvom		Manual
Parameter	width	spc	enc	spc	enc	spc	enc	spc	enc	spc	enc	merge?
hn-well	0.840	2.000	X	X	X	X	X	X	X	X	X	Yes
hvi	0.600	0.700	•	0.180	0.180	0.180	0.180	•	•	0.700	X	Yes
hd-iff	0.290	0.430	0.330	0.300	X	X	X	X	X	X	X	•
htap	0.150	0.430	0.330		•	0.270	X	X	X	X	X	•
HV poly	0.500	•	•	0.075	•	0.055	•	0.210	X	•	•	•

Manual merge means that features below min. space should be manually merged by drawing.

Table 5.25: Table F3c: Back end layers for S8D* flow

Layer	CD	licon		li1		mcon		meta		via		meta		via2		meta	
Parameter	width	spc	enc	spc	enc	spc	enc	spc	enc	spc	enc	spc	enc	spc	enc	spc	enc
li1	0.170	un-de-fined	0.000	0.170	X	X	X	X	X	X	X	X	X	X	X	X	X
mcon	0.170	•	•	•	0.000	0.190	X	X	X	X	X	X	X	X	X	X	X
meta	0.140	•	•	•	•	•	0.03/0.06	0.140	X	X	X	X	X	X	X	X	X
via	0.150	•	•	•	•	•	•	•	0.055/0.085	0.170	X	X	X	X	X	X	X
meta	0.140	•	•	•	•	•	•	•	•	•	0.055/0.085	0.140	X	X	X	X	X
via2	0.280	•	•	•	•	•	•	•	•	•	•	•	0.040	0.280	X	X	X
meta	0.360	•	•	•	•	•	•	•	•	•	•	•	•	•	0.045/0.07	0.360	X
	All enclosures in tables are nominal and do not apply to butting edges or corners.																

Table 5.26: Table F3d: Back end layers for S8T* flow

Layer	CD	li-con		li1		mcon		meta		via		meta		via2		meta	
Parameter	width	spc	enc	spc	enc	spc	enc	spc	enc	spc	enc	spc	enc	spc	enc	spc	enc
li1	0.170	un-de-fined	0.000	0.170	X	X	X	X	X	X	X	X	X	X	X	X	X
mcon	0.170	•	•	•	0.000	0.190	X	X	X	X	X	X	X	X	X	X	X
meta	0.140	•	•	•	•	•	0.03/0.06	0.140	X	X	X	X	X	X	X	X	X
via	0.150	•	•	•	•	•	•	•	0.055/0.085	0.170	X	X	X	X	X	X	X
meta	0.140	•	•	•	•	•	•	•	•	•	0.055	0.140	X	X	X	X	X
via2	0.280	•	•	•	•	•	•	•	•	•	•	•	0.190	1.200	X	X	X
meta	2.500	•	•	•	•	•	•	•	•	•	•	•	•	•	0.310	2.500	X
	All enclosures in tables are nominal and do not apply to butting edges or corners.																

Table 5.27: Table F4: Connectivity of Drawn and Mask Layers[Page 80, 1]

	Deep N Well	N Well	Diff	Tap	Poly	Li1	Capm	Met1	Met2	Met3	Met4	Met5	rdl
Deep N Well	N/A												
N Well	Over	N/A											
Diff	X	X	N/A										
Tap	X	Over	X	N/A									
Poly	X	X	X	X	N/A								
Li1	X	X	Li-con1	Li-con1	Li-con1 AND Npc	N/A							
Capm	X	X	X	X	X	X	N/A						
Met1	X	X	X	X	X	Mcon	X	N/A					
Met2	X	X	X	X	X	X	X	Via	N/A				
Met3	X	X	X	X	X	X	Via2	X	Via2	N/A			
Met4	X	X	X	X	X	X	X	X	X	Via3	N/A		
Met5	X	X	X	X	X	X	X	X	X	X	Via4	N/A	
rdl	X	X	X	X	X	X	X	X	X	X	X	(pad AND pmm) for s8pir/s8pr2-10r flows[Page 80, 1]	N/A
bump	X	X	X	X	X	X	X	X	X	X	X	X	pi2 AND ubm

Table 5.28: Table F5: Device Connectivity Table

Devices	LVS	Latch up	Soft
Transistors	open	open	open
resistor	open	open	open
diode	open	open	open
pnp	open	open	open
Inductor	open	short	open
capacitors	open	open	open

[1] All layers drawn except pmm which is created as cpmm:mask over bond pads or converted into cpbo:mask.

5.7 Periphery Rules

Use	Explanation
P	Rule applies to periphery only (outside areaid.ce). A corresponding core rule may or may not exist.
NE	Rule not checked for esd_nwell_tap. There are no corresponding rule for esd_nwell_tap.
NC	Rule not checked by DRC. It should be used as a guideline only.
TC	Rule not checked for cell name "*_tech_CD_top*"
A	Rule documents a functionality implemented in CL algorithms and may not be checked by DRC.
AD	Rule documents a functionality implemented in CL algorithms and checked by DRC.
DE	Rule not checked for source of Drain Extended device
LVS	Rule handled by LVS
F	Rule intended for Frame only, not checked inside Die
DNF	Drawn Not equal Final. The drawn rule does not reflect the final dimension on silicon. See table J for details.
RC	Recommended rule at the chip level, required rule at the IP level.
RR	Recommended rule at any IP level
AL	Rules applicable only to Al BE flows
CU	Rules applicable only to Cu BE flows
IR	IR drop check compering Al database and slotted Cu database for the same product (2 gds files) must be clean
EXEMPT	Rule is an exception?

5.7.1 (x.-)

Table 5.29: Function: Defines General (FIXME)

Name	Description	Flags	Value	Unit
(x.1a)	p1m.md (OPC), DECA and AMKOR layers (pi1.dg, pmm.dg, rdl.dg, pi2.dg, ubm.dg, bump.dg) and mask data for p1m, met1, via, met2 must be on a grid of mm		0.001	mm
(x.1b)	Data for SKY130 layout and mask on all layers except those mentioned in 1a must be on a grid of mm (except inside Seal ring)		0.005	mm
(x.2)	Angles permitted on: diff		N/A	N/A
(x.2)	**Angles permitted on: diff except for:** • diff inside "advSeal_6μm* OR cuPillarAdvSeal_6μm*" pcell, • diff rings around the die at min total L>1000 μm and W=0.3 μm		n x 90	deg

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Table 5.29 – continued from previous page

Name	Description	Flags	Value	Unit
(x.2)	Angles permitted on: tap (except inside areaid.en), poly (except for ESD flare gates or gated_npn), li1(periphery), licon1, capm, mcon, via, via2. Anchors are exempted.		n x 90	deg
(x.2)	Angles permitted on: via3 and via4. Anchors are exempted.		n x 90	deg
(x.2a)	Analog circuits identified by areaid.analog to use rectangular diff and tap geometries only; that are not to be merged into more complex shapes (T's or L's)			
(x.2c)	45 degree angles allowed on diff, tap inside UHVI			
(x.3)	Angles permitted on all other layers and in the seal ring for all the layers			
(x.3a)	Angles permitted on all other layers except WLCSP layers (pmm, rdl, pmm2, ubm and bump)		n x 45	deg
(x.4)	Electrical DR cover layout guidelines for electromigration	NC		
(x.5)	All "pin" polygons must be within the "drawing" polygons of the layer	AL		
(x.6)	All intra-layer separation checks will include a notch check			
(x.7)	Mask layer line and space checks must be done on all layers (checked with s.x rules)	NC		
(x.8)	Use of areaid "core" layer ("coreid") must be approved by technology	NC		
(x.9)	**Shapes on maskAdd or maskDrop layers ("serifs") are allowed in core only. Exempted are:** • cfom md/mp inside "advSeal_6um* OR cuPillarAdvSeal_6um*" pcell • diff rings around the die at min total L>1000 um and W=0.3 um, and PMM/PDMM inside areaid:sl			
(x.9)	Shapes on maskAdd or maskDrop layers ("serifs") are allowed in core only. PMM/PDMM inside areaid:sl are excluded.		N/A	N/A
(x.10)	Res purpose layer for (diff, poly) cannot overlap licon1			
(x.11)	Metal fuses are drawn in met2	LVS	N/A	N/A
(x.11)	Metal fuses are drawn in met3	LVS	N/A	N/A
(x.11)	Metal fuses are drawn in met4	LVS		
(x.n12ar	**To comply with the minimum spacing requirement for layer X in the frame:** • Spacing of areaid.mt to any non-ID layer • Enclosure of any non-ID layer by areaid.mt • Rules exempted for cells with name "*_buildspace"	F		
(x.12d)	Spacing of areaid.mt to huge_metX (Exempt met3.dg)	F	N/A	N/A
(x.12d)	Spacing of areaid.mt to huge_metX (Exempt met5.dg)	F		
(x.12e)	Enclosure of huge_metX by areaid.mt (Exempt met3.dg)	F	N/A	N/A
(x.12e)	Enclosure of huge_metX by areaid.mt (Exempt met5.dg)	F		
(x.13)	Spacing between features located across areaid:ce is checked by . . .			
(x.14)	Width of features straddling areaid:ce is checked by . . .			
(x.15a)	Drawn compatible, mask, and waffle-drop layers are allowed only inside areaid:mt (i.e., etest modules), or inside areaid:sl (i.e., between the outer and inner areaid:sl edges, but not in the die) or inside areaid:ft (i.e., frame, blankings). Exception: FOM/P1M/Metal waffle drop are allowed inside the die	P		
(x.15b)	Rule X.15a exempted for cpmm.dg inside cellnames "PadPLfp", "padPLhp", "padPLstg" and "padPLwlbi" (for the SKY130di-5r-gsmc flow)	EX-EMPT		
(x.16)	Die must not overlap areaid.mt (rule waived for test chips and exempted for cell-names "*tech_CD_*", "*_techCD_*", "lazX_*" or "lazY_*")			

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Table 5.29 – continued from previous page

Name	Description	Flags	Value	Unit
(x.17)	All labels must be within the "drawing" polygons of the layer; This check is enabled by using switch "floating_labels"; Identifies floating labels which appear as warnings in LVS. Using this check would enable cleaner LVS run; Not a gate for tapeout			
(x.18)	Use redundant mcon, via, via2, via3 and via4 (Locations where additional vias/contacts can be added to existing single vias/contacts will be identified by this rule). Single via under areaid.core and areaid.standarc are excluded from the single via check	RR		
(x.19)	Lower left corner of the seal ring should be at origin i.e (0,0)			
(x.20)	Min spacing between pins on the same layer (center to center); Check enabled by switch "IP_block"			
(x.21)	prunde.dg is allowed only inside areaid.mt or areaid.sc			
(x.22)	No floating interconnects (poly, li1, met1-met5) or capm allowed; Rule flags interconnects with no path to poly, difftap or metal pins. Exempt floating layers can be excluded using poly_float, li1_float, m1_float, m2_float, m3_float, m4_float and m5_float text labels. Also flags an error if these text labels are placed on connected layers (not floating) and if the labels are not over the appropriate metal layer. If floating interconnects need to be connected at a higher level (Parent IP or Full chip), such floating interconnects can be exempted using poly_tie, li1_tie, m1_tie, m2_tie, m3_tie, m4_tie and m5_tie text labels. It is the responsibility of the IP owner and chip/product owner to communicate and agree to the node each of these texted lines is connected to, if there is any risk to how a line is tied, and to what node. Only metals outside areaid.stdcell are checked. The following are exempt from x.22 violations: _techCD_ , inductor.dg, modulecut, capacitors and s8blerf The 'notPublicCell' switch will deactivate this rule	RC		
(x.23a)	areaid.sl must not overlap diff		N/A	N/A
(x.23b)	diff cannot straddle areaid.sl			
(x.23c)	areaid.sl must not overlap tap, poly, li1 and metX			
(x.23d)	areaid.sl must not overlap tap, poly		N/A	N/A
(x.23e)	areaid:sl must not overlap li1 and metX for pcell "advSeal_6um"		N/A	N/A
(x.23f)	areaid:SubstrateCut (areaid.st, local_sub) must not straddle p+ tap	RR		
(x.24)	condiode label must be in iso_pwell			
(x.25)	pnp.dg must be only within cell name "s8rf_pnp", "s8rf_pnp5x" or "s8tesd_iref_pnp", "stk14ecx_*"			
(x.26)	"advSeal_6um" pcell must overlap diff			
(x.27)	If the sealring is present, then partnum is required. To exempt the requirement, place text.dg saying "partnum_not_necessary". "partnum*block" pcell should be used instead of "partnum*" pcells	RR	N/A	N/A
(x.28)	Min width of areaid.sl		N/A	N/A
(x.29)	nfet must be enclosed by dnwell. Rule is checked when switch nfet_in_dnwell is turned on.			

5.7.2 (dnwell.-)

Table 5.30: Function: Define deep nwell for isolating pwell and noise immunity

Name	Description	Flags	Value	Unit
(dnwell.2	Min width of deep nwell		3.000	μm
(dnwell.3	Min spacing between deep nwells. Rule exempt inside UHVI.		6.300	μm
(dnwell.3	Min spacing between deep nwells on same net inside UHVI.		N/A	N/A
(dnwell.3	Min spacing between deep-nwells inside UHVI and deep-nwell outside UHVI		N/A	N/A
(dnwell.3	Min spacing between deep-nwells inside UHVI and nwell outsideUHVI		N/A	N/A
(dnwell.3	Min spacing between deep-nwells inside UHVI on different nets		N/A	N/A
(dnwell.4	Dnwell can not overlap pnp:dg			
(dnwell.5	P+_diff can not straddle Dnwell			
(dnwell.6	RF NMOS must be enclosed by deep nwell (RF FETs are listed in $DE-SIGN/config/tech/model_set/calibre/fixed_layout_model_map of corresponding techs)			
(dnwell.7	Dnwell can not straddle areaid:substratecut			

5.7.3 (nwell.-)

Table 5.31: Function: Define nwell implant regions

Name	Description	Flags	Value	Unit
(nwell.1)	Width of nwell		0.840	μm
(nwell.2a	Spacing between two n-wells		1.270	μm
(nwell.2b	Manual merge wells if less than minimum			
(nwell.4)	All n-wells will contain metal-contacted tap (rule checks only for licon on tap) . Rule exempted from high voltage cells inside UHVI			
(nwell.5)	Deep nwell must be enclosed by nwell by atleast… Exempted inside UHVI or areaid.lw Nwells can merge over deep nwell if spacing too small (as in rule nwell.2)	TC	0.400	μm
(nwell.5a	min enclosure of nwell by dnwell inside UHVI		N/A	N/A
(nwell.5b	nwell inside UHVI must not be on the same net as nwell outside UHVI		N/A	N/A
(nwell.6)	Min enclosure of nwell hole by deep nwell outside UHVI	TC	1.030	μm
(nwell.7)	Min spacing between nwell and deep nwell on separate nets Spacing between nwell and deep nwell on the same net is set by the sum of the rules nwell.2 and nwell.5. By default, DRC run on a cell checks for the separate-net spacing, when nwell and deep nwell nets are separate within the cell hierarchy and are joined in the upper hierarchy. To allow net names to be joined and make the same-net rule applicable in this case, the "joinNets" switch should be turned on. waffle_chip	TC	4.500	μm
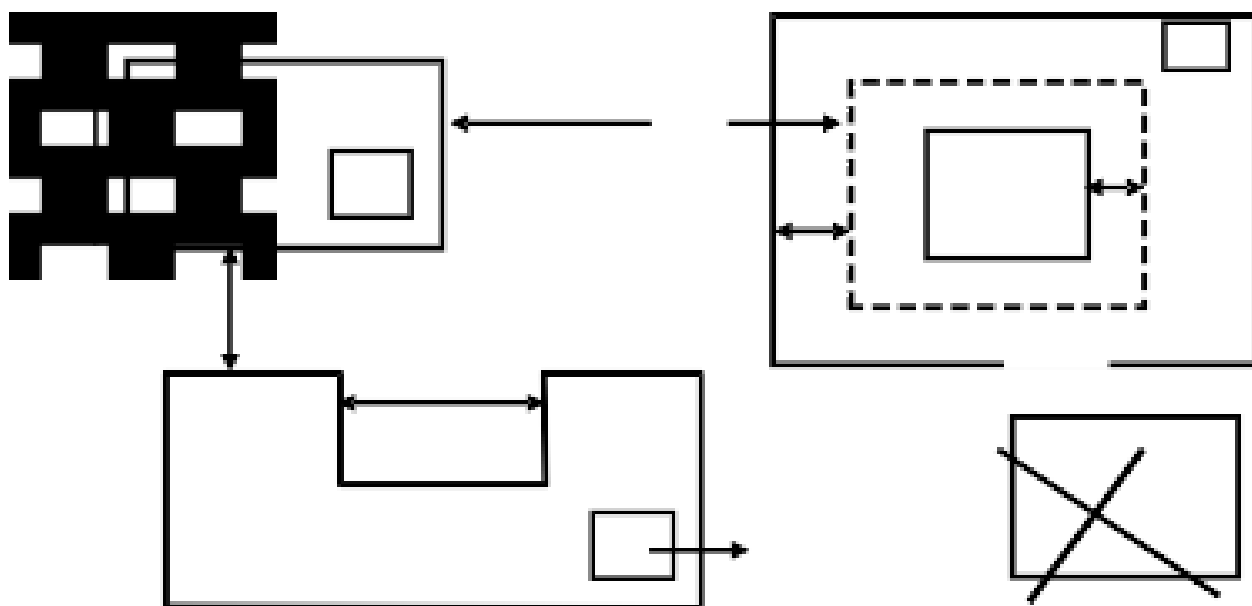
5.7.4 (pwbm.-)

Table 5.32: Function: Define p-well block

Name	Description	Flags	Value	Unit
(pwbm.1	Min width of pwbm.dg		N/A	N/A
(pwbm.2	Min spacing between two pwbm.dg inside UHVI		N/A	N/A
(pwbm.3	Min enclosure of dnwell:dg by pwbm.dg inside UHVI (exempt pwbm hole inside dnwell)		N/A	N/A
(pwbm.4	dnwell inside UHVI must be enclosed by pwbm (exempt pwbm hole inside dnwell)		N/A	N/A
(pwbm.5	Min Space between two pwbm holes inside UHVI		N/A	N/A

5.7.5 (pwdem.-)

Table 5.33: Function: Defines Pwdem (FIXME)

Name	Description	Flags	Value	Unit
(pwdem.1)	Min width of pwdem.dg		N/A	N/A
(pwdem.2)	Min spacing between two pwdem.dg inside UHVI on same net		N/A	N/A
(pwdem.3)	Min enclosure of pwdem:dg by pwbm.dg inside UHVI		N/A	N/A
(pwdem.4)	pwdem.dg must be enclosed by UHVI		N/A	N/A
(pwdem.5)	pwdem.dg inside UHVI must be enclosed by deep nwell		N/A	N/A
(pwdem.6)	Min enclosure of pwdem:dg by deep nwell inside UHVI		N/A	N/A
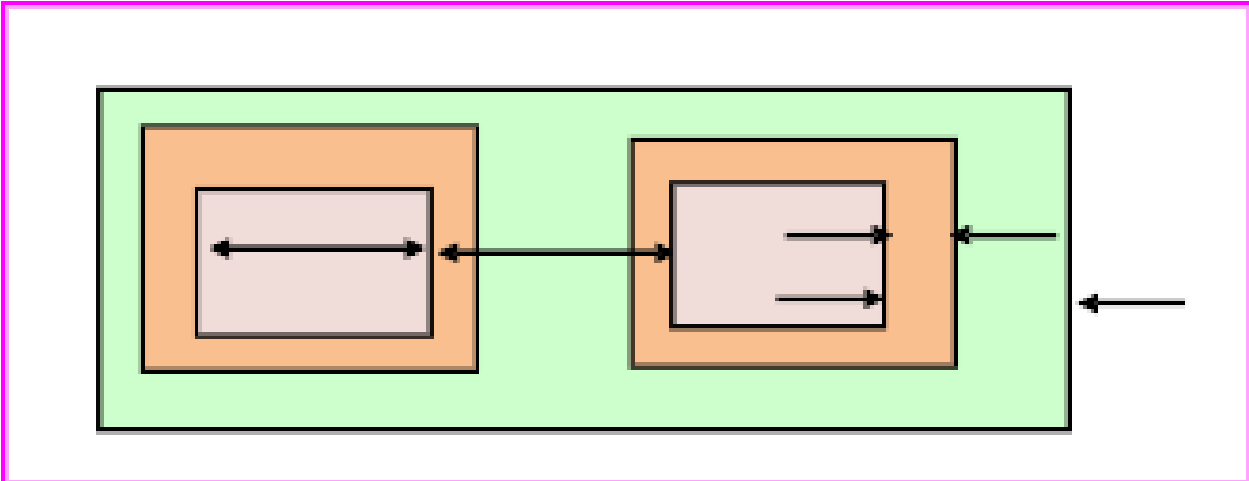
5.7.6 (hvtp.-)

Table 5.34: Function: Define Vt adjust implant region for high Vt LV
PMOS;

Name	Description	Flags	Value	Unit
(hvtp.1)	Min width of hvtp		0.380	μm
(hvtp.2)	Min spacing between hvtp to hvtp		0.380	μm
(hvtp.3)	Min enclosure of pfet by hvtp	P	0.180	μm
(hvtp.4)	Min spacing between pfet and hvtp	P	0.180	μm
(hvtp.5)	Min area of hvtp		0.265	μm²
(hvtp.6)	Min area of hvtp Holes		0.265	μm²
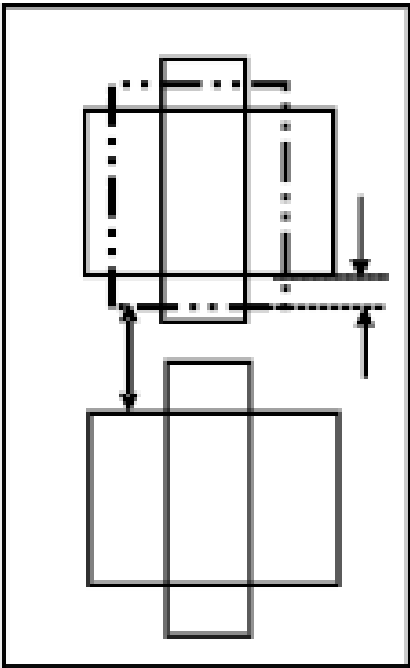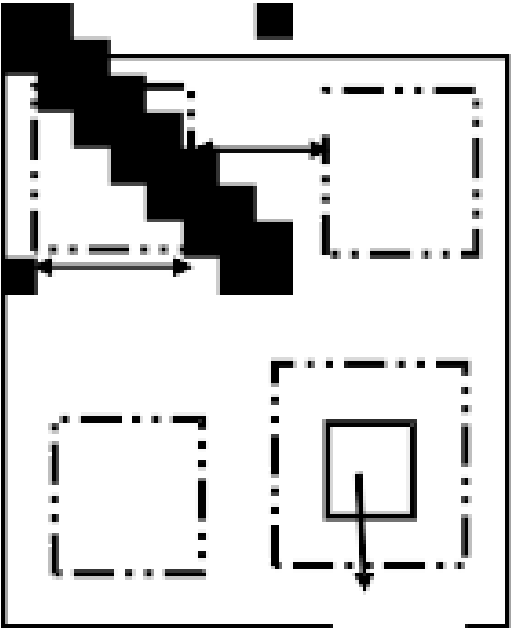
5.7.7 (hvtr.-)

Table 5.35: Function: Define low VT adjust implant region for pmedlvtrf;

Name	Description	Flags	Value	Unit
(hvtr.1)	Min width of hvtr		0.380	μm
(hvtr.2)	Min spacing between hvtp to hvtr		0.380	μm
(hvtr.3)	Min enclosure of pfet by hvtr	P	0.180	μm

5.7.8 (lvtn.-)

Table 5.36: Function: Define regions to block Vt adjust implant for low
Vt LV PMOS/NMOS, SONOS FETs and Native NMOS

Name	Description	Flags	Value	Unit
(lvtn.1a)	Min width of lvtn		0.380	μm
(lvtn.2)	Min space lvtn to lvtn		0.380	μm
(lvtn.3a)	Min spacing of lvtn to gate. Rule exempted inside UHVI.	P	0.180	μm
(lvtn.3b)	Min spacing of lvtn to pfet along the S/D direction	P	0.235	μm
(lvtn.4b)	Min enclosure of gate by lvtn. Rule exempted inside UHVI.	P	0.180	μm
(lvtn.9)	Min spacing, no overlap, between lvtn and hvtp		0.380	μm
(lvtn.10)	Min enclosure of lvtn by (nwell not overlapping Var_channel) (exclude coincident edges)		0.380	μm
(lvtn.12)	Min spacing between lvtn and (nwell inside areaid.ce)		0.380	μm
(lvtn.13)	Min area of lvtn		0.265	μm^2
(lvtn.14)	Min area of lvtn Holes		0.265	μm^2
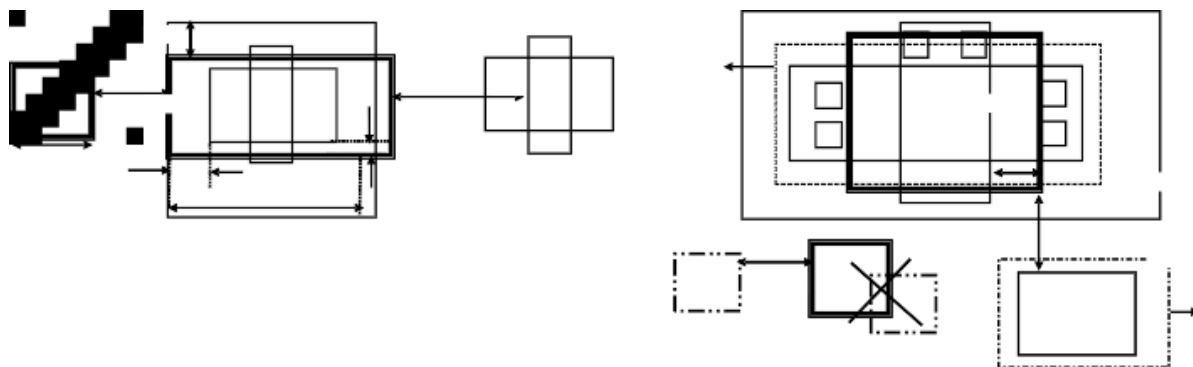
5.7.9 (ncm.-)

Table 5.37: Function: Define Vt adjust implant region for LV NMOS in the core of NVSRAM

Name	Description	Flags	Value	Unit
(ncm.X.2	Ncm overlapping areaid:ce is checked for core rules only			
(ncm.X.3	Ncm overlapping core cannot overlap N+diff in periphery	TC		
(ncm.1)	Width of ncm		0.380	µm
(ncm.2a	Spacing of ncm to ncm		0.380	µm
(ncm.2b	Manual merge ncm if space is below minimum			
(ncm.3)	Min enclosure of P+diff by Ncm	P	0.180	µm
(ncm.4)	Min enclosure of P+diff within (areaid:ed AndNot areaid:de) by Ncm	P	0.180	µm
(ncm.5)	Min space, no overlap, between ncm and (LVTN_gate) OR (diff containing lvtn)	P	0.230	µm
(ncm.6)	Min space, no overlap, between ncm and nfet	P	0.200	µm
(ncm.7)	Min area of ncm		0.265	µm^2
(ncm.8)	Min area of ncm Holes		0.265	µm^2
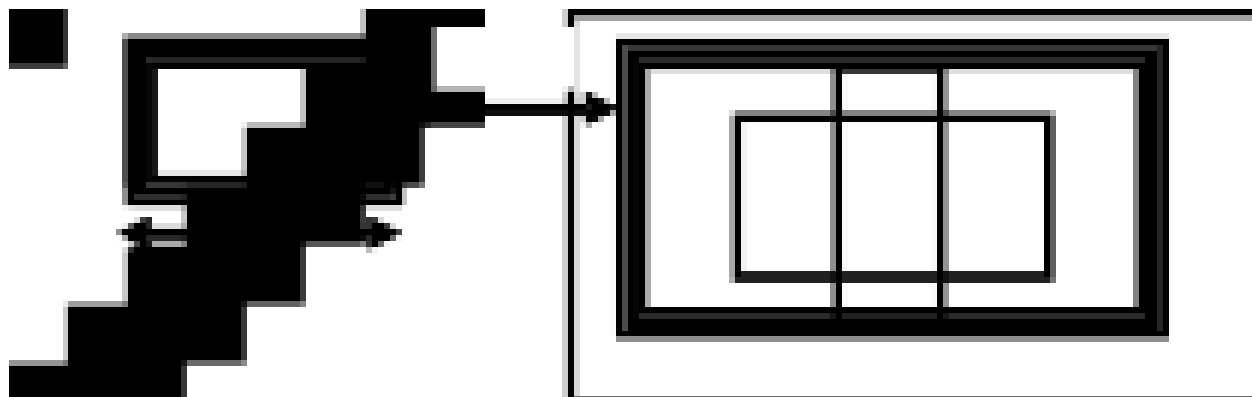
5.7.10 (difftap.-)

Table 5.38: Function: Defines active regions and contacts to substrate

Name	Description	Flags	Value	Unit
(diff-tap.1)	Width of diff or tap	P	0.150	µm
(diff-tap.2)	Minimum channel width (Diff And Poly) except for FETs inside areaid.sc: Rule exempted in the SP8* flows only, for the cells listed in rule difftap.2a	P	0.420	µm
(diff-tap.2a)	Minimum channel width (Diff And Poly) for cell names "s8cell_ee_plus_sseln_a", "s8cell_ee_plus_sseln_b", "s8cell_ee_plus_sselp_a", "s8cell_ee_plus_sselp_b" , "s8fpls_pl8", "s8fpls_rdrv4" , "s8fpls_rdrv4f" and "s8fpls_rdrv8"	P	NA	µm
(diff-tap.2b)	Minimum channel width (Diff And Poly) for FETs inside areaid.sc	P	0.360	µm
(diff-tap.3)	Spacing of diff to diff, tap to tap, or non-abutting diff to tap		0.270	µm
(diff-tap.4)	Min tap bound by one diffusion		0.290	
(diff-tap.5)	Min tap bound by two diffusions	P	0.400	
(diff-tap.6)	Diff and tap are not allowed to extend beyond their abutting edge			
(diff-tap.7)	Spacing of diff/tap abutting edge to a non-conciding diff or tap edge	NE	0.130	µm
(diff-tap.8)	Enclosure of (p+) diffusion by N-well. Rule exempted inside UHVI.	DE NE P	0.180	µm
(diff-tap.9)	Spacing of (n+) diffusion to N-well outside UHVI	DE NE P	0.340	µm
(diff-tap.10)	Enclosure of (n+) tap by N-well. Rule exempted inside UHVI.	NE P	0.180	µm
(diff-tap.11)	Spacing of (p+) tap to N-well. Rule exempted inside UHVI.		0.130	µm
(diff-tap.12)	ESD_nwell_tap is considered shorted to the abutting diff	NC		
(diff-tap.13)	Diffusion or the RF FETS in Table H5 is defined by Ldiff and Wdiff.			

5.7.11 (tunm.-)

Table 5.39: Function: Defines SONOS FETs

Name	Description	Flags	Value	Unit
(tunm.1)	Min width of tunm		0.410	μm
(tunm.2)	Min spacing of tunm to tunm		0.500	μm
(tunm.3)	Extension of tunm beyond (poly and diff)		0.095	
(tunm.4)	Min spacing of tunm to (poly and diff) outside tunm		0.095	μm
(tunm.5)	(poly and diff) may not straddle tunm			
(tunm.6a	Tunm outside deep n-well is not allowed	TC		
(tunm.7)	Min tunm area		0.672	μm^2
(tunm.8)	tunm must be enclosed by areaid.ce			
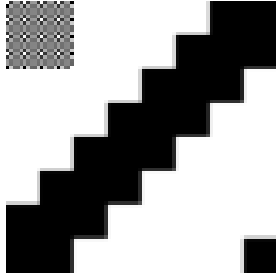
5.7.12 (poly.-)

Table 5.40: Function: Defines FET gates, interconnects and resistors

Name	Description	Flags	Value	Unit
(poly.X.1	All FETs would be checked for W/Ls as documented in spec 001-02735 (Exempt FETs that are pruned; exempt for W/L's inside areaid.sc and inside cell name scs8*decap* and listed in the MRGA as a decap only W/L)			
(poly.X.1	Min & max dummy_poly L is equal to min L allowed for corresponding device type (exempt rule for dummy_poly in cells listed on Table H3)			
(poly.1a)	Width of poly		0.150	µm
(poly.1b)	Min channel length (poly width) for pfet overlapping lvtn (exempt rule for dummy_poly in cells listed on Table H3)		0.350	µm
(poly.2)	Spacing of poly to poly except for poly.c2 and poly.c3; Exempt cell: sr_bltd_eq where it is same as poly.c2		0.210	µm
(poly.3)	Min poly resistor width		0.330	µm
(poly.4)	Spacing of poly on field to diff (parallel edges only)	P	0.075	µm
(poly.5)	Spacing of poly on field to tap	P	0.055	µm
(poly.6)	Spacing of poly on diff to abutting tap (min source)	P	0.300	µm
(poly.7)	Extension of diff beyond poly (min drain)	P	0.250	
(poly.8)	Extension of poly beyond diffusion (endcap)	P	0.130	
(poly.9)	Poly resistor spacing to poly or spacing (no overlap) to diff/tap		0.480	µm
(poly.10)	Poly can't overlap inner corners of diff			
(poly.11)	No 90 deg turns of poly on diff			
(poly.12)	(Poly NOT (nwell NOT hvi)) may not overlap tap; Rule exempted for cell name "s8fgvr_n_fg2" and gated_npn and inside UHVI.	P		
(poly.15)	Poly must not overlap diff:rs			
(poly.16)	Inside RF FETs defined in Table H5, poly cannot overlap poly across multiple adjacent instances			
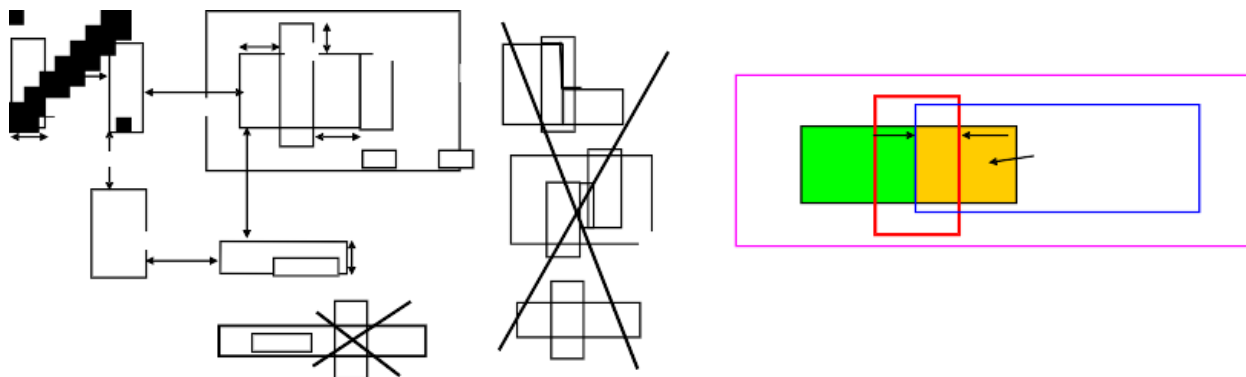
5.7.13 (rpm.-)

Table 5.41: Function: Defines p+ poly resistors

Name	Description	Flags	Value	Unit
(rpm.1a)	Min width of rpm		1.270	µm
(rpm.1b)	Min/Max prec_resistor width xhrpoly_0p35		0.350	µm
(rpm.1c)	Min/Max prec_resistor width xhrpoly_0p69		0.690	µm
(rpm.1d)	Min/Max prec_resistor width xhrpoly_1p41		1.410	µm
(rpm.1e)	Min/Max prec_resistor width xhrpoly_2p85		2.850	µm
(rpm.1f)	Min/Max prec_resistor width xhrpoly_5p73		5.730	µm
(rpm.1g)	Only 1 licon is allowed in xhrpoly_0p35 prec_resistor_terminal			
(rpm.1h)	Only 1 licon is allowed in xhrpoly_0p69 prec_resistor_terminal			
(rpm.1i)	Only 2 licons are allowed in xhrpoly_1p41 prec_resistor_terminal			
(rpm.1j)	Only 4 licons are allowed in xhrpoly_2p85 prec_resistor_terminal			
(rpm.1k)	Only 8 licons are allowed in xhrpoly_5p73 prec_resistor_terminal			
(rpm.2)	Min spacing of rpm to rpm		0.840	µm
(rpm.3)	rpm must enclose prec_resistor by atleast		0.200	
(rpm.4)	prec_resistor must be enclosed by psdm by atleast		0.110	µm
(rpm.5)	prec_resistor must be enclosed by npc by atleast		0.095	µm
(rpm.6)	Min spacing, no overlap, of rpm and nsdm		0.200	µm
(rpm.7)	Min spacing between rpm and poly		0.200	µm
(rpm.8)	poly must not straddle rpm			
(rpm.9)	Min space, no overlap, between prec_resistor and hvntm		0.185	µm
(rpm.10)	Min spacing of rpm to pwbm		N/A	N/A
(rpm.11)			N/A	N/A
	rpm should not overlap or straddle pwbm except cells			
	s8usbpdv2_csa_top			
	s8usbpdv2_20vconn_sw_300ma_ovp_ngate_unit			
	s8usbpdv2_20vconn_sw_300ma_ovp			
	s8usbpdv2_20sbu_sw_300ma_ovp			
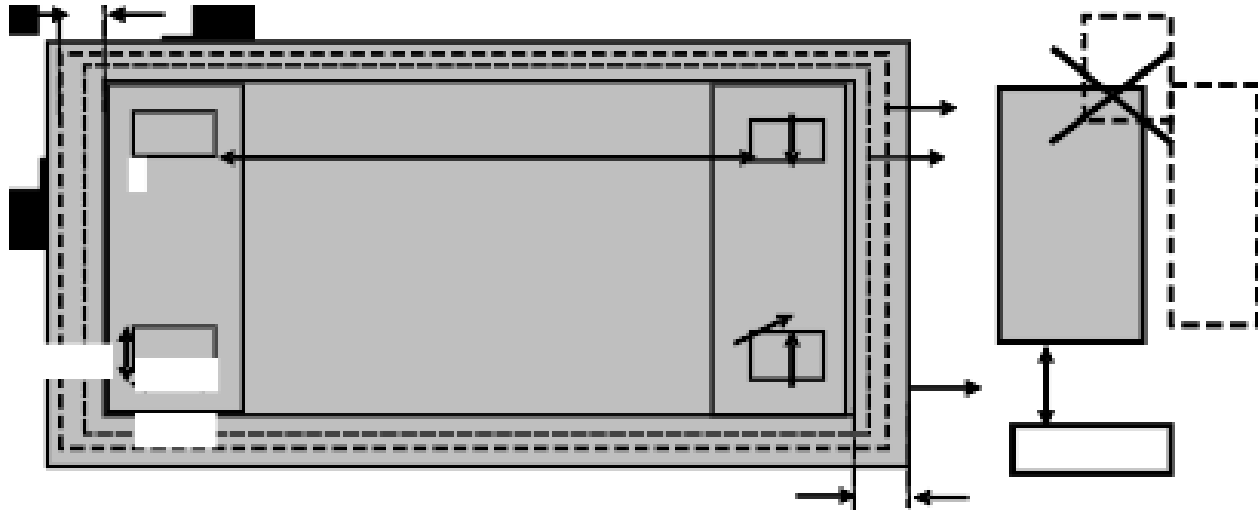
5.7.14 (varac.-)

Table 5.42: Function: Defines varactors

Name	Description	Flags	Value	Unit
(varac.1	Min channel length (poly width) of Var_channel		0.180	µm
(varac.2	Min channel width (tap width) of Var_channel		1.000	µm
(varac.3	Min spacing between hvtp to Var_channel		0.180	µm
(varac.4	Min spacing of licon on tap to Var_channel		0.250	µm
(varac.5	Min enclosure of poly overlapping Var_channel by nwell		0.150	µm
(varac.6	Min spacing between VaracTap and difftap		0.270	µm
(varac.7	Nwell overlapping Var_channel must not overlap P+ diff			
(varac.8	Min enclosure of Var_channel by hvtp		0.255	µm

5.7.15 (photo.-)

Table 5.43: Function: Photo diode for sensing light

Name	Description	Flags	Value	Unit
(photo.1	Rules dnwell.3 and nwell.5 are exempted for photoDiode			
(photo.2	Min/Max width of photoDiode		3.000	µm
(photo.3	Min spacing between photoDiode		5.000	µm
(photo.4	Min spacing between photoDiode and deep nwell		5.300	µm
(photo.5	photoDiode edges must be coincident with areaid.po			
(photo.6	photoDiode must be enclosed by dnwell ring			
(photo.7	photoDiode must be enclosed by p+ tap ring			
(photo.8	Min/Max width of nwell inside photoDiode		0.840	µm
(photo.9	Min/Max enclosure of nwell by photoDiode		1.080	µm
(photo.1	Min/Max width of tap inside photoDiode		0.410	µm
(photo.1	Min/Max enclosure of tap by nwell inside photoDiode		0.215	µm
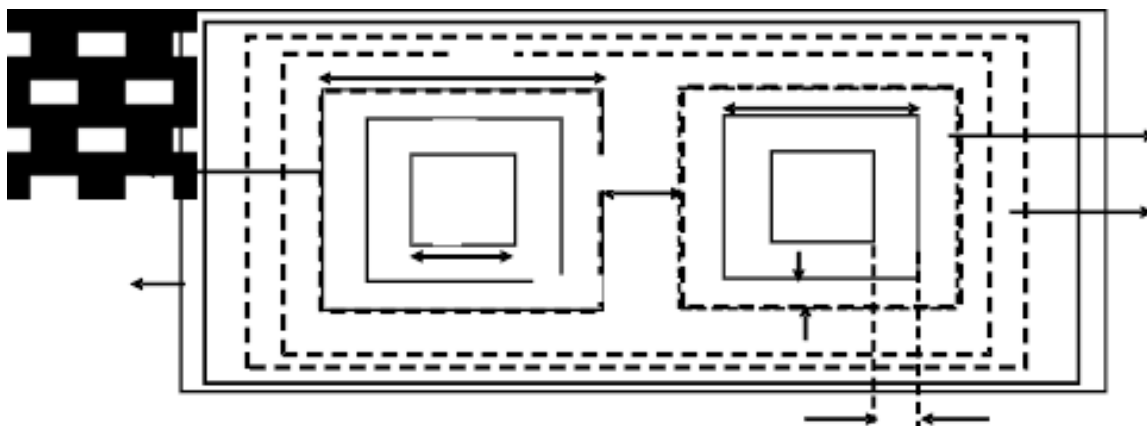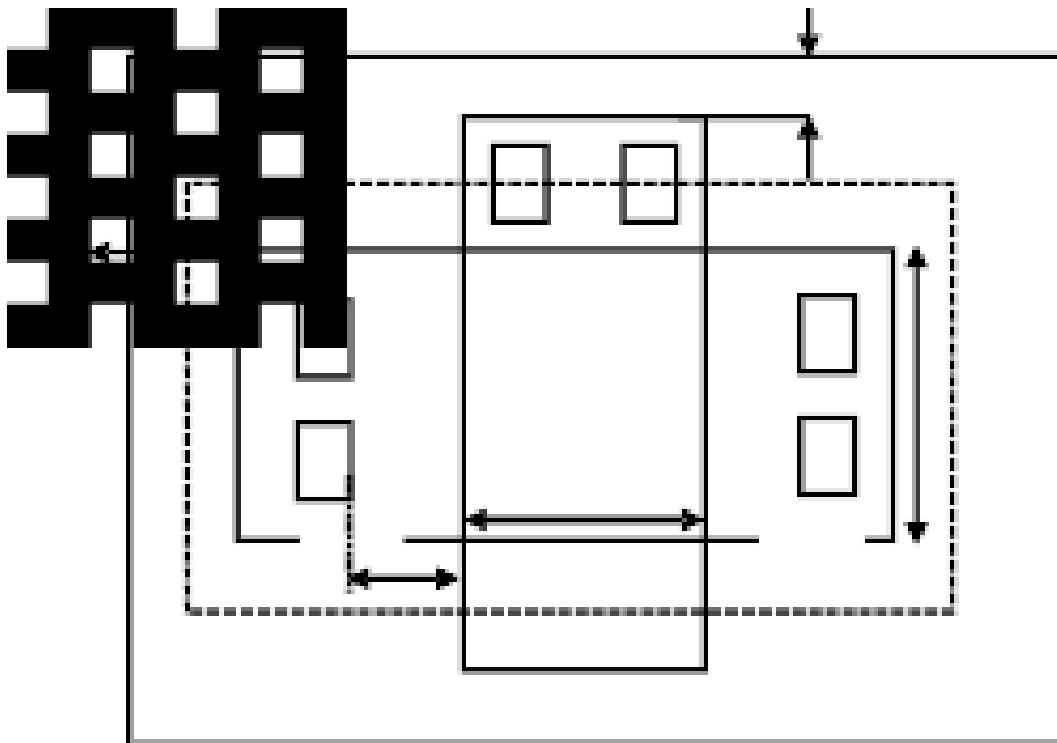
5.7.16 (npc.-)

Table 5.44: Function: Defines nitride openings to contact poly and Li1

Name	Description	Flags	Value	Unit
(npc.1)	Min width of NPC		0.270	µm
(npc.2)	Min spacing of NPC to NPC		0.270	µm
(npc.3)	Manual merge if less than minimum			
(npc.4)	Spacing (no overlap) of NPC to Gate		0.090	µm
(npc.5)	Max enclosure of poly overlapping slotted_licon by npcm (merge between adjacent short edges of the slotted_licons if space < min)		0.095	µm
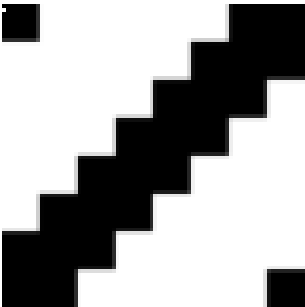
5.7.17 (n/ psd.-)

Table 5.45: Function: Defines opening for N+/P+ implants

Name	Description	Flags	Value	Unit
(n/ psd.1)	Width of nsdm(psdm)	P	0.380	μm
(n/ psd.2)	Spacing of nsdm(psdm) to nsdm(psdm)	P	0.380	μm
(n/ psd.3)	Manual merge if less than minimum			
(n/ psd.5a)	Enclosure of diff by nsdm(psdm), except for butting edge		0.125	μm
(n/ psd.5b)	Enclosure of tap by nsdm(psdm), except for butting edge	P	0.125	μm
(n/ psd.6)	Enclosure of diff/tap butting edge by nsdm (psdm)		0.000	μm
(n/ psd.7)	Spacing of NSDM/PSDM to opposite implant diff or tap (for non-abutting diff/tap edges)		0.130	μm
(n/ psd.8)	Nsdm and psdm cannot overlap diff/tap regions of opposite doping	DE		
(n/ psd.9)	**Diff and tap must be enclosed by their corresponding implant layers. Rule exempted for** • diff inside "advSeal_6um* OR cuPillarAdvSeal_6um*" pcell for SKY130P*/SP8P*/SKY130DI-5R-CSMC flows • diff rings around the die at min total L>1000 um and W=0.3 um • gated_npn • areaid.zer.	DE		
(n/ psd.10a	Min area of Nsdm		0.265	μm^2
(n/ psd.10b	Min area of Psdm		0.255	μm^2
(n/ psd.11)	Min area of n/psdmHoles		0.265	μm^2

5.7.18 (licon.-)

Table 5.46: Function: Defines contacts between poly/diff/tap and Li1

Name	Description	Flags	Value	Unit
(li-con.1)	Min and max L and W of licon (exempt licons inside prec_resistor)		0.170	µm
(li-con.1b)	Min and max width of licon inside prec_resistor		0.190	µm
(li-con.1c)	Min and max length of licon inside prec_resistor		2.000	µm
(li-con.2)	Spacing of licon to licon	P	0.170	µm
(li-con.2b)	Min spacing between two slotted_licon (when the both the edges are 0.19um in length)		0.350	µm
(li-con.2c)	Min spacing between two slotted_licon (except for rule licon.2b)		0.510	µm
(li-con.2d)	Min spacing between a slotted_licon and 0.17um square licon		0.510	µm
(li-con.3)	Only min. square licons are allowed except die seal ring where licons are (licon CD)*L		0.170 *L	
(li-con.4)	Licon1 must overlap li1 and (poly or diff or tap)			
(li-con.5a)	Enclosure of licon by diff	P	0.040	µm
(li-con.5b)	Min space between tap_licon and diff-abutting tap edge	P	0.060	µm
(li-con.5c)	Enclosure of licon by diff on one of two adjacent sides	P	0.060	µm
(li-con.6)	Licon cannot straddle tap	P		
(li-con.7)	Enclosure of licon by one of two adjacent edges of isolated tap	P	0.120	µm
(li-con.8)	Enclosure of poly_licon by poly	P	0.050	µm
(li-con.8a)	Enclosure of poly_licon by poly on one of two adjacent sides	P	0.080	µm
(li-con.9)	Spacing, no overlap, between poly_licon and psdm; In SKY130DIA/SKY130TMA/SKY130PIR-10 flows, the rule is checked only between (poly_licon outside rpm) and psdm	P	0.110	µm
(li-con.10)	Spacing of licon on (tap AND (nwell NOT hvi)) to Var_channel	P	0.250	µm
(li-con.11)	Spacing of licon on diff or tap to poly on diff (except for all FETs inside areaid.sc and except s8spf-10r flow for 0.5um phv inside cell names "s8fs_gwdlvx4", "s8fs_gwdlvx8", "s8fs_hvrsw_x4", "s8fs_hvrsw8", "s8fs_hvrsw264", and "s8fs_hvrsw520" and for 0.15um nshort inside cell names "s8fs_rdecdrv", "s8fs_rdec8", "s8fs_rdec32", "s8fs_rdec264", "s8fs_rdec520")	P	0.055	µm
(li-con.11a	Spacing of licon on diff or tap to poly on diff (for all FETs inside areaid.sc except 0.15um phighvt)	P	0.050	µm
(li-con.11b	Spacing of licon on diff or tap to poly on diff (for 0.15um phighvt inside areaid.sc)	P	0.050	µm

Table 5.46 – continued from previous page

Name	Description	Flags	Value	Unit
(li-con.11c)	Spacing of licon on diff or tap to poly on diff (for 0.5um phv inside cell names "s8fs_gwdlvx4", "s8fs_gwdlvx8", "s8fs_hvrsw_x4", "s8fs_hvrsw8", "s8fs_hvrsw264", and "s8fs_hvrsw520")	P	0.040	μm
(li-con.11d)	Spacing of licon on diff or tap to poly on diff (for 0.15um nshort inside cell names "s8fs_rdecdrv", "s8fs_rdec8", "s8fs_rdec32", "s8fs_rdec264", "s8fs_rdec520")	P	0.045	μm
(li-con.12)	Max SD width without licon	NC	5.700	μm
(li-con.13)	Spacing (no overlap) of NPC to licon on diff or tap	P	0.090	μm
(li-con.14)	Spacing of poly_licon to diff or tap	P	0.190	μm
(li-con.15)	poly_licon must be enclosed by npc by…	P	0.100	μm
(li-con.16)	Every source_diff and every tap must enclose at least one licon1, including the diff/tap straddling areaid:ce. Rule exempted inside UHVI.	P		
(li-con.17)	Licons may not overlap both poly and (diff or tap)			
(li-con.18)	Npc must enclose poly_licon			
(li-con.19)	poly of the HV varactor must not interact with licon	P		

5.7.19 (li.-.-)

Table 5.47: Function: Defines local interconnect to diff/tap and poly

Name	Description	Flags	Value	Unit
(li.1.-)	Width of LI (except for li.1a)	P	0.170	μm
(li.1a.-)	Width of LI inside of cells with name s8rf2_xcmvpp_hd5_*	P	0.140	μm
(li.2.-)	Max ratio of length to width of LI without licon or mcon	NC	10.00	μm
(li.3.-)	Spacing of LI to LI (except for li.3a)	P	0.170	μm
(li.3a.-)	Spacing of LI to LI inside cells with names s8rf2_xcmvpp_hd5_*	P	0.140	μm
(li.5.-)	Enclosure of licon by one of two adjacent LI sides	P	0.080	μm
(li.6.-)	Min area of LI	P	0.056	μm^2
(li.7.-)	Min LI resistor width (rule exempted within areaid.ed; Inside areaid.ed, min width of the li resistor is determined by rule li.1)		0.290	μm
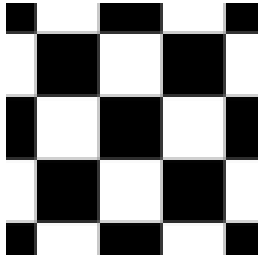
5.7.20 (ct.-)

Table 5.48: Function: Defines contact between Li1 and met1

Name	Description	Flags	Value	Unit
(ct.1)	Min and max L and W of mcon	DNF	0.170	µm
(ct.2)	Spacing of mcon to mcon	DNF	0.190	µm
(ct.3)	Only min. square mcons are allowed except die seal ring where mcons are…		0.170	
(ct.4)	Mcon must be enclosed by LI by at least …	P	0.000	µm
(ct.irdrop	For 1 <= n <= 10 contacts on the same connector, mcon area pre- and post- Cu conversion must differ by no more than…	CU IR	0.2	µm
(ct.irdrop	For 11 <= n <= 100 contacts on the same connector, mcon area pre- and post- Cu conversion must differ by no more than…	CU IR	0.3	µm
(ct.irdrop	For n > 100 contacts on the same connector, mcon area pre- and post- Cu conversion must differ by no more than…	CU IR	0.7	µm

5.7.21 (capm.-)

Table 5.49: Function: Defines MIM capacitor

Name	Description	Flags	Value	Unit
(capm.1	Min width of capm		N/A	N/A
(capm.2	Min spacing of capm to capm		N/A	N/A
(capm.2	Minimum spacing of capacitor bottom_plate to bottom plate		N/A	N/A
(capm.3	Minimum enclosure of capm (top_plate) by met2		N/A	N/A
(capm.4	Min enclosure of via2 by capm		N/A	N/A
(capm.5	Min spacing between capm and via2		N/A	N/A
(capm.6	Maximum Aspect Ratio (Length/Width)		N/A	N/A
(capm.7	Only rectangular capacitors are allowed		N/A	N/A
(capm.8	Min space, no overlap, between via and capm		N/A	N/A
(capm.1	capm must not straddle nwell, diff, tap, poly, li1 and met1 (Rule exempted for capm overlapping capm_2t.dg)	TC	N/A	N/A
(capm.1	Min spacing between capm to (met2 not overlapping capm)		N/A	N/A
(capm.1	Max area of capm (um^2)		N/A	N/A

5.7.22 (vpp.-)

Table 5.50: Function: Defines VPP capacitor

Name	Description	Flags	Value	Unit
(vpp.1)	Min width of capacitor:dg		1.430	μm
(vpp.1b)	Max width of capacitor:dg; Rule not applicable for vpp_with_Met3Shield and vpp_with_LiShield and vpp_over_MOSCAP and vpp_with_Met5 and vpp_with_noLi		11.35	μm
(vpp.1c)	Min/Max width of cell name "s8rf_xcmvpp1p8x1p8_m3shield "		3.880	μm
(vpp.3)	capacitor:dg must not overlap (tap or diff or poly); (one exception: Poly is allowed to overlap vpp_with_Met3Shield and vpp_with_Met5PolyShield); (not applicable for vpp_over_Moscap or "s8rf2_xcmvppx4_2xnhvnative10x4" or vpp_with_LiShield)			
(vpp.4)	capacitor:dg must not straddle (nwell or dnwell)			
(vpp.5)	Min spacing between (capacitor:dg edge and (poly or li1 or met1 or met2)) to (poly or li1 or met1 or met2) on separate nets (Exempt area of the error shape less than 2.25 μm^2 and run length less than 2.0um); Rule not applicable for vpp_with_Met3Shield and vpp_with_LiShield and vpp_over_MOSCAP and vpp_with_Met5 and vpp_with_noLi		1.500	μm
(vpp.5a)	Max pattern density of met3.dg over capacitor.dg (not applicable for vpp_with_Met3Shield and vpp_with_LiShield and vpp_over_MOSCAP and vpp_with_Met5)		0.25	-
(vpp.5b)	Max pattern density of met4.dg over capacitor.dg (not applicable for vpp_with_Met3Shield and vpp_with_Met5 and vpp_over_MOSCAP)		0.3	-
(vpp.5c)	Max pattern density of met5.dg over capacitor.dg (not applicable for vpp_with_Met3Shield and vpp_with_Met5 and vpp_over_MOSCAP and vpp_with_noLi); (one exception: rules does apply to cell "s8rf2_xcmvpp11p5x11p7_m1m4" and "s8rf2_xcmvpp_hd5_atlas*")		0.4	-
(vpp.8)	Min enclosure of capacitor:dg by nwell		1.500	μm
(vpp.9)	Min spacing of capacitor:dg to nwell (not applicable for vpp_over_MOSCAP)		1.500	μm
(vpp.10)	vpp capacitors must not overlap; Rule checks for capacitor.dg overlapping more than one pwell pin			
(vpp.11)	Min pattern density of (poly and diff) over capacitor.dg; (vpp_over_Moscap only)		0.87	-
(vpp.12a	Number of met4 shapes inside capacitor.dg of cell "s8rf2_xcmvpp8p6x7p9_m3_lim5shield" must overlap with size 2.01 x 2.01 (no other met4 shapes allowed)		9.00	μm
(vpp.12b	Number of met4 shapes inside capacitor.dg of cell "s8rf2_xcmvpp11p5x11p7_m3_lim5shield" must overlap with size 2.01 x 2.01 (no other met4 shapes allowed)		16.00	μm
(vpp.12c	Number of met4 shapes inside capacitor.dg of cell "s8rf2_xcmvpp4p4x4p6_m3_lim5shield" must overlap with size 1.5 x 1.5 (no other met4 shapes allowed)		4.00	μm
(vpp.13)	Min space of met1 to met1inside VPP capacitor	CU	0.160	μm
(vpp.14)	Min space of met2 to met2 inside VPP capacitor	CU	0.160	μm
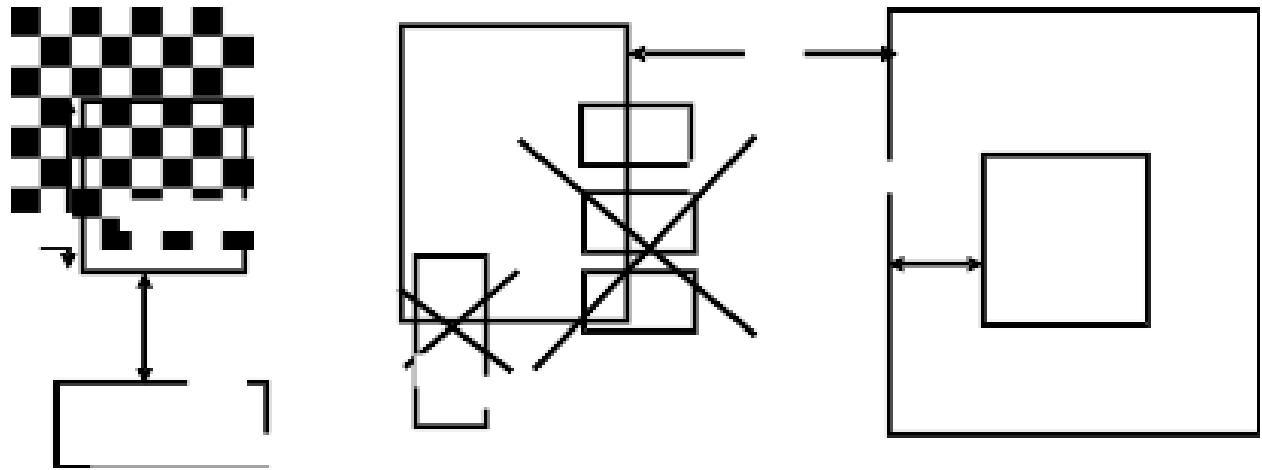
5.7.23 (m1.-)

Table 5.51: Function: Defines first level of metal interconnects, buses
etc;

Name	Description	Flags	Value	Unit
(m1.-)		RC		
	Algorithm should flag errors, for met1, if ANY of the following is true:			
	An entire 700x700 window is covered by cmm1 waffleDrop, and metX PD < 70% for same window.			
	80-100% of 700x700 window is covered by cmm1 waffleDrop, and metX PD < 65% for same window.			
	60-80% of 700x700 window is covered by cmm1 waffleDrop, and metX PD < 60% for same window.			
	50-60% of 700x700 window is covered by cmm1 waffleDrop, and metX PD < 50% for same window.			
	40-50% of 700x700 window is covered by cmm1 waffleDrop, and metX PD < 40% for same window.			
	30-40% of 700x700 window is covered by cmm1 waffleDrop, and metX PD < 30% for same window.			
	Exclude cells whose area is below 40Kum2. NOTE: Required for IP, Recommended for Chip-level.			
(m1.1)	Width of metal1		0.140	µm
(m1.2)	Spacing of metal1 to metal1		0.140	µm
(m1.3a)	Min. spacing of features attached to or extending from huge_met1 for a distance of up to 0.280 µm to metal1 (rule not checked over non-huge met1 features)		0.280	µm
(m1.3b)	Min. spacing of huge_met1 to metal1 excluding features checked by m1.3a		0.280	µm
(m1.4)	Mcon must be enclosed by Met1 by at least …(Rule exempted for cell names documented in rule m1.4a)	P	0.030	µm
(m1.4a)	Mcon must be enclosed by Met1 by at least (for cell names "s8cell_ee_plus_sseln_a", "s8cell_ee_plus_sseln_b", "s8cell_ee_plus_sselp_a", "s8cell_ee_plus_sselp_b", "s8fpls_pl8", and "s8fs_cmux4_fm")	P	0.005	µm
(m1.5)	Mcon must be enclosed by Met1 on one of two adjacent sides by at least …	P AL	0.060	µm
(m1.6)	Min metal 1 area		0.083	µm²
(m1.7)	Min area of metal1 holes		0.140	µm²
(m1.pd.1	Min MM1_oxide_Pattern_density	RR AL	0.7	-
(m1.pd.2	Rule m1.pd.1 has to be checked by dividing the chip into square regions of width and length equal to …	A AL	700	µm
(m1.pd.2	Rule m1.pd.1 has to be checked by dividing the chip into steps of …	A AL	70	
(m1.11)	Max width of metal1after slotting	CU NC	4.000	µm
(m1.12)	Add slots and remove vias and contacts if met1 wider than…..	CU	3.200	
(m1.13)	Max pattern density (PD) of met1	CU	0.77	-
(m1.14)	Met1 PD window size	CU	50.00	µm
(m1.14a	Met1 PD window step	CU	25.00	µm
(m1.15)	Mcon must be enclosed by met1 on one of two adjacent sides by at least …	CU	0.030	µm

5.7.24 (via.-)

Table 5.52: Function: Defines contact between met1 and met2

Name	Description	Flags	Value	Unit
(via.1a)	Min and max L and W of via outside areaid.mt	AL	0.150	µm
(via.1b)	Three sizes of square Vias allowed inside areaid:mt: 0.150um, 0.230um and 0.280um	AL		
(via.2)	Spacing of via to via	AL	0.170	µm
(via.3)	Only min. square vias are allowed except die seal ring where vias are (Via CD)*L		0.2*L	
(via.4a)	0.150 µm Via must be enclosed by Met1 by at least …		0.055	µm
(via.4b)	Inside areaid.mt, 0.230 µm Via must be enclosed by met1 by atleast	AL	0.030	µm
(via.4c)	Inside areaid.mt, 0.280 µm Via must be enclosed by met1 by atleast	AL	0.000	µm
(via.5a)	0.150 µm Via must be enclosed by Met1 on one of two adjacent sides by at least …		0.085	µm
(via.5b)	Inside areaid.mt, 0.230 µm Via must be enclosed by met1 on one of two adjacent sides by at least …	AL	0.060	µm
(via.5c)	Inside areaid.mt, 0.280 µm Via must be enclosed by met1 on one of two adjacent sides by at least …	AL	0.000	µm
(via.11)	Min and max L and W of via outside areaid.mt	CU	0.180	µm
(via.12)	Min spacing between vias	CU	0.130	µm
(via.13)	Max of 5 vias within …	CU	0.350	µm
(via.14)	0.180 µm Via must be enclosed by parallel edges of Met1 by at least …	CU	0.040	µm
(via.irdrc	For 1 <= n <= 2 vias on the same connector, mcon area pre- and post- Cu conversion must differ by no more than…	CU IR	0.0	µm
(via.irdrc	For 3 <= n <= 15 vias on the same connector, mcon area pre- and post- Cu conversion must differ by no more than…	CU IR	0.6	µm
(via.irdrc	For 16 <= n <= 30 vias on the same connector, mcon area pre- and post- Cu conversion must differ by no more than…	CU IR	0.8	µm
(via.irdrc	For n > 30 vias on the same connector, mcon area pre- and post- Cu conversion must differ by no more than…	CU IR	0.9	µm
(via.14a	0.180 µm Via must be enclosed by 45 deg edges of Met1 by at least …	CU	0.037	deg µm
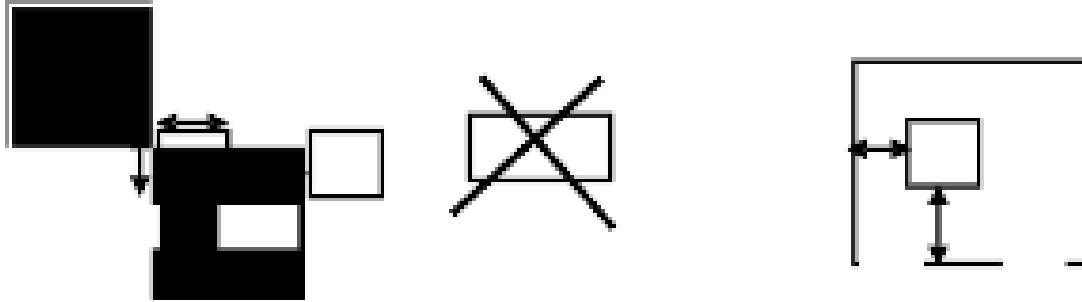
5.7.25 (m2.-)

Table 5.53: Function: Defines second level of metal interconnects, buses etc

Name	Description	Flags	Value	Unit
(m2.-)		RC		
	Algorithm should flag errors, for met2, if ANY of the following is true:			
	An entire 700x700 window is covered by cmm2 waffleDrop, and metX PD < 70% for same window.			
	80-100% of 700x700 window is covered by cmm2 waffleDrop, and metX PD < 65% for same window.			
	60-80% of 700x700 window is covered by cmm2 waffleDrop, and metX PD < 60% for same window.			
	50-60% of 700x700 window is covered by cmm2 waffleDrop, and metX PD < 50% for same window.			
	40-50% of 700x700 window is covered by cmm2 waffleDrop, and metX PD < 40% for same window.			
	30-40% of 700x700 window is covered by cmm2 waffleDrop, and metX PD < 30% for same window.			
	Exclude cells whose area is below 40Kum2. Required for IP, Recommended for Chip-level.			
(m2.1)	Width of metal 2		0.140	μm
(m2.2)	Spacing of metal 2 to metal 2		0.140	μm
(m2.3a)	Min. spacing of features attached to or extending from huge_met2 for a distance of up to 0.280 μm to metal2 (rule not checked over non-huge met2 features)		0.280	μm
(m2.3b)	Min. spacing of huge_met2 to metal2 excluding features checked by m2.3a		0.280	μm
(m2.3c)	Min spacing between floating_met2 with AR_met2_A >= 0.05 and AR_met2_B =< 0.032, outside areaid:sc must be greater than	RR	0.145	μm
(m2.4)	Via must be enclosed by Met2 by at least …	P AL	0.055	μm
(m2.5)	Via must be enclosed by Met2 on one of two adjacent sides by at least …	AL	0.085	μm
(m2.6)	Min metal2 area		0.067	μm^2
(m2.7)	Min area of metal2 holes		0.140	μm^2
(m2.pd.1	Min MM2_oxide_Pattern_density	RR	0.7	-
(m2.pd.2	Rule m2.pd.1 has to be checked by dividing the chip into square regions of width and length equal to …	A	700	μm
(m2.pd.2	Rule m2.pd.1 has to be checked by dividing the chip into steps of …	A	70	
(m2.11)	Max width of metal2	CU	4.000	μm
(m2.12)	Add slots and remove vias and contacts if met2 wider than…..	CU	3.200	
(m2.13)	Max pattern density (PD) of metal2	CU	0.77	-
(m2.14)	Met2 PD window size	CU	50.00	μm
(m2.14a	Met2 PD window step	CU	25.00	μm
(m2.15)	Via must be enclosed by met2 by at least…	CU	0.040	μm

5.7.26 (via2.-)

Table 5.54: Function: Via2 connects met2 to met3 in the SKY130T*/SKY130P*/SP8Q/SP8P* flows and met2/capm to met3 in the SKY130DI* flow.

Name	Description	Flags	Value	Unit
(via2.X.)	Via2 connects met2 to met3 in the SKY130T*/SKY130P*/SP8Q/SP8P* flow and met2/capm to met3 in the SKY130DI* flow.			
(via2.1a)	Min and max L and W of via2 (except for rule via2.1b/1c/1d/1e/1f)	AL	0.200	µm
(via2.1b)	Three sizes of square Vias allowed inside areaid:mt: 0.280um, 1.2 um and 1.5 um	AL	N/A	N/A
(via2.1c)	Two sizes of square Vias allowed inside areaid:mt: 1.2 um and 1.5 um	AL	N/A	N/A
(via2.1d)	Four sizes of square Vias allowed inside areaid:mt: 0.2um, 0.280um, 1.2 um and 1.5 um	AL		
(via2.1e)	Three sizes of square Vias allowed inside areaid:mt: 0.8um, 1.2 um and 1.5 um	AL	N/A	N/A
(via2.1f)	Two sizes of square Vias allowed outside areaid:mt: 0.8um and 1.2 um	AL	N/A	N/A
(via2.2)	Spacing of via2 to via2	AL	0.200	µm
(via2.3)	Only min. square via2s are allowed except die seal ring where via2s are (Via2 CD)*L	AL	0.2*L	
(via2.4)	Via2 must be enclosed by Met2 by at least …	AL	0.040	µm
(via2.4a)	Inside areaid.mt, 1.5 µm Via2 must be enclosed by met2 by atleast		0.140	µm
(via2.5)	Via2 must be enclosed by Met2 on one of two adjacent sides by at least …	AL	0.085	µm
(via2.11)	Min and max L and W of via2	CU	0.210	µm
(via2.12)	Min spacing between via2's	CU	0.180	µm
(via2.13)	Min spacing between via2 rows	CU	0.200	µm
(via2.14)	Via2 must be enclosed by met2 by atleast	CU	0.035	µm
(via2.ird)	For 1 <= n <= 2 via2's on the same connector, mcon area pre- and post- Cu conversion must differ by no more than…	CU IR	0.0	µm
(via2.ird)	For 3 <= n <= 4 via2's on the same connector, mcon area pre- and post- Cu conversion must differ by no more than…	CU IR	0.6	µm
(via2.ird)	For 5 <= n <= 30 via2's on the same connector, mcon area pre- and post- Cu conversion must differ by no more than…	CU IR	0.79	µm
(via2.ird)	For n > 30 via2's on the same connector, mcon area pre- and post- Cu conversion must differ by no more than…	CU IR	0.9	µm
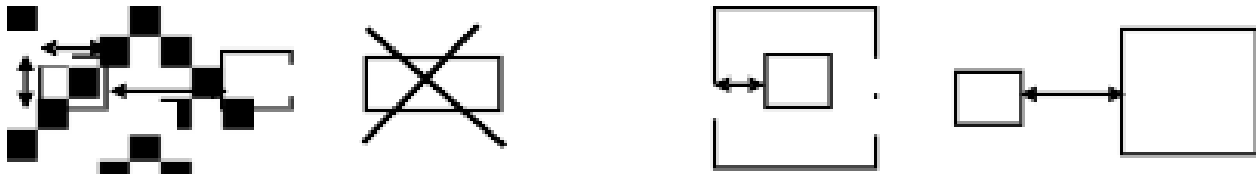
5.7.27 (m3.-)

Table 5.55: Function: Defines third level of metal interconnects, buses etc

Name	Description	Flags	Value	Unit
(m3.-)		RC		
	Algorithm should flag errors, for met3, if ANY of the following is true:			
	An entire 700x700 window is covered by cmm3 waffleDrop, and metX PD < 70% for same window.			
	80-100% of 700x700 window is covered by cmm3 waffleDrop, and metX PD < 65% for same window.			
	60-80% of 700x700 window is covered by cmm3 waffleDrop, and metX PD < 60% for same window.			
	50-60% of 700x700 window is covered by cmm3 waffleDrop, and metX PD < 50% for same window.			
	40-50% of 700x700 window is covered by cmm3 waffleDrop, and metX PD < 40% for same window.			
	30-40% of 700x700 window is covered by cmm3 waffleDrop, and metX PD < 30% for same window.			
	Exclude cells whose area is below 40Kum2. NOTE: Required for IP, Recommended for Chip-level.			
(m3.1)	Width of metal 3		0.300	μm
(m3.2)	Spacing of metal 3 to metal 3		0.300	μm
(m3.3a)	Min. spacing of features attached to or extending from huge_met3 for a distance of up to 0.480 um to metal3 (rule not checked over non-huge met3 features)		N/A	N/A
(m3.3b)	Min. spacing of huge_met3 to metal3 excluding features checked by m3.3a		N/A	N/A
(m3.3c)	Min. spacing of features attached to or extending from huge_met3 for a distance of up to 0.400 μm to metal3 (rule not checked over non-huge met3 features)		0.400	μm
(m3.3d)	Min. spacing of huge_met3 to metal3 excluding features checked by m3.3a		0.400	μm
(m3.4)	Via2 must be enclosed by Met3 by at least …	AL	0.065	μm
(m3.5)	Via2 must be enclosed by Met3 on one of two adjacent sides by at least …		N/A	N/A
(m3.5a)	Via2 must be enclosed by Met3 on all sides by at least …(Rule not checked on a layout when it satisfies both rules m3.4 and m3.5)		N/A	N/A
(m3.6)	Min area of metal3		0.240	μm^2
(m3.7)	Min area of metal3 holes	CU	0.200	μm^2
(m3.pd.1	Min MM3_oxide_Pattern_density	RR	0.7	-
(m3.pd.2	Rule m3.pd.1 has to be checked by dividing the chip into square regions of width and length equal to …	A	700	μm
(m3.pd.2	Rule m3.pd.1 has to be checked by dividing the chip into steps of …	A	70	
(m3.11)	Max width of metal3	CU	4.000	μm
(m3.12)	Add slots and remove vias and contacts if wider than…..	CU	3.200	
(m3.13)	Max pattern density (PD) of metal3	CU	0.77	-
(m3.14)	Met3 PD window size	CU	50.00	μm
(m3.14a	Met3 PD window step	CU	25.00	μm
(m3.15)	Via2 must be enclosed by met3 by at least…	CU	0.060	μm

5.7.28 (via3.-)

Table 5.56: Function: Via3 connects met3 to met4 in the SKY130Q*/SKY130P*/SP8Q/SP8P* flow

Name	Description	Flags	Value	Unit
(via3.1)	Min and max L and W of via3 (except for rule via3.1a)	AL	0.200	μm
(via3.1a	Two sizes of square via3 allowed inside areaid.mt: 0.200um and 0.800um	AL		
(via3.2)	Spacing of via3 to via3	AL	0.200	μm
(via3.3)	Only min. square via3s are allowed except die seal ring where via3s are (Via3 CD)*L		0.2*L	
(via3.4)	Via3 must be enclosed by Met3 by at least …	AL	0.060	μm
(via3.5)	Via3 must be enclosed by Met3 on one of two adjacent sides by at least …	AL	0.090	μm
(via3.11	Min and max L and W of via3	CU	0.210	μm
(via3.12	Min spacing between via2's	CU	0.180	μm
(via3.13	Via3 must be enclosed by Met3 by at least …	CU	0.055	μm
(via3.14	Min spacing between via3 rows	CU	0.350	μm
(via3.ird	For 1 <= n <= 2 via3's on the same connector, mcon area pre- and post- Cu conversion must differ by no more than…	CU IR	0.0	μm
(via3.ird	For 3 <= n <= 15 via3's on the same connector, mcon area pre- and post- Cu conversion must differ by no more than…	CU IR	0.6	μm
(via3.ird	For 16 <= n <= 30 via3's on the same connector, mcon area pre- and post- Cu conversion must differ by no more than…	CU IR	0.8	μm
(via3.ird	For n > 30 via3's on the same connector, mcon area pre- and post- Cu conversion must differ by no more than…	CU IR	0.9	μm

5.7.29 (nsm.-)

Table 5.57: Function: Defines Nitride Seal Mask (FIXME)

Name	Description	Flags	Value	Unit
(nsm.1)	Min. width of nsm		3.000	µm
(nsm.2)	Min. spacing of nsm to nsm		4.000	µm
(nsm.3)	Min spacing, no overlap, between NSM_keepout to diff.dg, tap.dg, fom.dy, cfom.dg, cfom.mk, poly.dg, p1m.mk, li1.dg, cli1m.mk, metX.dg (X=1 to 5) and cmmX.mk (X=1 to 5). Exempt the following from the check: (a) cell name "nikon*" and (b) diff ring inside areaid.sl	AL	1.000	µm
(nsm.3a	Min enclosure of diff.dg, tap.dg, fom.dy, cfom.dg, cfom.mk, poly.dg, p1m.mk, li1.dg, cli1m.mk, metX.dg (X=1 to 5) and cmmX.mk (X=1 to 5) by areaid.ft. Exempt the following from the check: (a) cell name "s8Fab_crntic*" (b) blankings in the frame (rule uses areaid.dt for exemption)		3.000	µm
(nsm.3b	Min spacing between areaid.dt to diff.dg, tap.dg, fom.dy, cfom.dg, cfom.mk, poly.dg, p1m.mk, li1.dg, cli1m.mk, metX.dg (X=1 to 5) and cmmX.mk (X=1 to 5). Exempt the following from the check: (a) blankings in the frame (rule uses areaid.dt for exemption)		3.000	µm

5.7.30 (indm.-)

Table 5.58: Function: Defines third level of metal interconnects, buses and inductor; top_indmMetal is met3 for SKY130D* flows; Similarly top_padVia is Via2 for SKY130D*

Name	Description	Flags	Value	Unit
(indm.1)	Min width of top_indmMetal		N/A	N/A
(indm.2)	Min spacing between two top_indmMetal		N/A	N/A
(indm.3)	top_padVia must be enclosed by top_indmMetal by atleast		N/A	N/A
(indm.4)	Min area of top_indmMetal		N/A	N/A
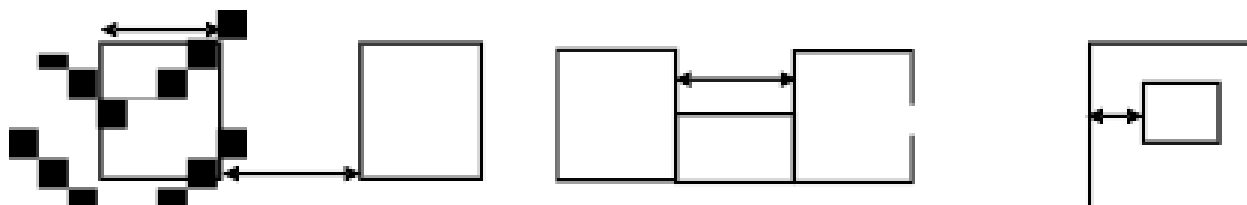
5.7.31 (m4.-)

Table 5.59: Function: Defines Fourth level of metal interconnects;

Name	Description	Flags	Value	Unit
(m4.-)		RC		
	Algorithm should flag errors, for met4, if ANY of the following is true:			
	An entire 700x700 window is covered by cmm4 waffleDrop, and metX PD < 70% for same window.			
	80-100% of 700x700 window is covered by cmm4 waffleDrop, and metX PD < 65% for same window.			
	60-80% of 700x700 window is covered by cmm4 waffleDrop, and metX PD < 60% for same window.			
	50-60% of 700x700 window is covered by cmm4 waffleDrop, and metX PD < 50% for same window.			
	40-50% of 700x700 window is covered by cmm4 waffleDrop, and metX PD < 40% for same window.			
	30-40% of 700x700 window is covered by cmm4 waffleDrop, and metX PD < 30% for same window.			
	Exclude cells whose area is below 40Kum2. Required for IP, Recommended for Chip-level.			
(m4.1)	Min width of met4		0.300	µm
(m4.2)	Min spacing between two met4		0.300	µm
(m4.3)	via3 must be enclosed by met4 by atleast	AL	0.065	µm
(m4.4)	Min area of met4 (rule exempted for probe pads which are exactly 1.42um by 1.42um)		N/A	N/A
(m4.4a)	Min area of met4		0.240	µm^2
(m4.5a)	Min. spacing of features attached to or extending from huge_met4 for a distance of up to 0.400 µm to metal4 (rule not checked over non-huge met4 features)		0.400	µm
(m4.5b)	Min. spacing of huge_met4 to metal4 excluding features checked by m4.5a		0.400	µm
(m4.7)	Min area of meta4 holes	CU	0.200	µm^2
(m4.pd.1	Min MM4_oxide_Pattern_density	RR	0.7	-
(m4.pd.2	Rule m4.pd.1 has to be checked by dividing the chip into square regions of width and length equal to …	A	700	µm
(m4.pd.2	Rule m4.pd.1 has to be checked by dividing the chip into steps of …	A	70	
(m4.11)	Max width of metal4	CU	10.00	µm
(m4.12)	Add slots and remove vias and contacts if wider than…..	CU	10.00	
(m4.13)	Max pattern density (PD) of metal4; met4 overlapping pdm areas are excluded from the check	CU	0.77	-
(m4.14)	Met4 PD window size	CU	50.00	µm
(m4.14a	Met4 PD window step	CU	25.00	µm
(m4.15)	Via3 must be enclosed by met4 by at least…	CU	0.060	µm
(m4.16)	Min enclosure of pad by met4	CU	0.850	µm

5.7.32 (via4.-)

Table 5.60: Function: Via4 connects met4 to met5 in the SKY130P*/SP8P* flow

Name	Description	Flags	Value	Unit
(via4.1)	Min and max L and W of via4		0.800	μm
(via4.2)	Spacing of via4 to via4		0.800	μm
(via4.3)	Only min. square via4s are allowed except die seal ring where via4s are (Via4 CD)*L		0.8*L	
(via4.4)	Via4 must be enclosed by Met4 by at least …		0.190	μm
(via4.ird	For 1 <= n <= 4 via4's on the same connector, mcon area pre- and post- Cu conversion must differ by no more than…	CU IR	0.0	μm
(via4.ird	For 5 <= n <= 10 via4's on the same connector, mcon area pre- and post- Cu conversion must differ by no more than…	CU IR	0.2	μm
(via4.ird	For 11 <= n <= 100 via4's on the same connector, mcon area pre- and post- Cu conversion must differ by no more than…	CU IR	0.5	μm
(via4.ird	For n > 100 via4's on the same connector, mcon area pre- and post- Cu conversion must differ by no more than…	CU IR	0.8	μm

5.7.33 (m5.-)

Table 5.61: Function: Defines Fifth level of metal interconnects;

Name	Description	Flags	Value	Unit
(m5.1)	Min width of met5		1.600	μm
(m5.2)	Min spacing between two met5		1.600	μm
(m5.3)	via4 must be enclosed by met5 by atleast		0.310	μm
(m5.4)	Min area of met5 (For all flows except SKY130PIR*/SKY130PF*, the rule is exempted for probe pads which are exactly 1.42um by 1.42um)		4.000	μm²

5.7.34 (pad.-)

Table 5.62: Function: Opens the passivation

Name	Description	Flags	Value	Unit
(pad.2)	Min spacing of pad:dg to pad:dg		1.270	μm
(pad.3)	Max area of hugePad NOT top_metal		30000	μm²

5.7.35 (rdl.-)

Table 5.63: Function: Defines the Cu Inductor. Connects to met5 through the pad opening

Name	Description	Flags	Value	Unit
(rdl.1)	Min width of rdl		10	μm
(rdl.2)	Min spacing between two rdl		10	μm
(rdl.3)	Min enclosure of pad by rdl, except rdl interacting with bump		10.75	μm
(rdl.4)	Min spacing between rdl and outer edge of the seal ring		15.00	μm
(rdl.5)	(rdl OR ccu1m.mk) must not overlap areaid.ft. Exempt the following from the check: (a) blankings in the frame (rule uses areaid.dt for exemption)			
(rdl.6)	Min spacing of rdl to pad, except rdl interacting with bump		19.66	μm

5.7.36 (mf.-)

Note: For SKY130D* and SKY130TM* CADflow use MM2 for Metal Fuse

For SP8P*/SKY130P* (PLM) CADflow use MM4 for Metal Fuse

Table 5.64: Function: Defines metal fuses

Name	Description	Flags	Value	Unit
(mf.1)	Min. and max width of fuse		0.800	µm
(mf.2)	Length of fuse		7.200	µm
(mf.3)	Spacing between centers of adjacent fuses		2.760	µm
(mf.4)	Spacing between center of fuse and fuse_metal (fuse shields are exempted)		3.300	µm
(mf.5)	Max. extension of fuse_metal beyond fuse boundary		0.830	
(mf.6)	Spacing (no overlapping) between fuse center and Metal1		3.300	µm
(mf.7)	Spacing (no overlapping) between fuse center and LI		3.300	µm
(mf.8)	Spacing (no overlapping) between fuse center and poly		2.660	µm
(mf.9)	Spacing (no overlapping) between fuse center and tap		2.640	µm
(mf.10)	Spacing (no overlapping) between fuse center and diff		3.250	µm
(mf.11)	Spacing (no overlapping) between fuse center and nwell		3.320	µm
(mf.12)	Size of fuse_shield		0.5x2	µm
(mf.13)	Min. spacing of center of fuse to fuse_shield		2.200	µm
(mf.14)	Max. spacing of center of fuse to fuse_shield		3.300	µm
(mf.15)	Fuse_shields are only placed between periphery metal (i.e., without fuse:dg) and non-isolated edges of fuse as defined by mf.16			
(mf.16)	The edge of a fuse is considered non-isolated if wider than or equal to mf.2 and spaced to fuse_metal by less than …		4.000	
(mf.17)	Offset between fuse_shields center and fuse center	NC	0.000	
(mf.18)	Min and max space between fuse_shield and fuse_metal (opposite edges). Rule checked within 1 gridpoint.		0.600	µm
(mf.19)	Spacing (no overlapping) between fuse center and Metal2		3.300	µm
(mf.20)	Only one fuse per metal line allowed			
(mf.21)	Min spacing , no overlap, between metal3 and fuse center		3.300	µm
(mf.22)	Min spacing between fuse_contact to fuse_contact		1.960	µm
(mf.23)	Spacing (no overlapping) between fuse center and Metal4		N/A	N/A
(mf.24)	Spacing (no overlapping) between fuse center and Metal5		3.300	µm

5.7.37 (hvi.-)

Table 5.65: Function: Defines thick oxide for high voltage devices

Name	Description	Flags	Value	Unit
(hvi.1)	Min width of Hvi	P	0.600	μm
(hvi.2a)	Min spacing of Hvi to Hvi	P	0.700	μm
(hvi.2b)	Manual merge if space is below minimum			
(hvi.4)	Hvi must not overlap tunm			
(hvi.5)	Min space between hvi and nwell (exclude coincident edges)		0.700	μm

5.7.38 (hvnwell.-)

Table 5.66: Function: Defines rules for HV nwell; All nwell connected to voltages greater than 1.8V must be enclosed by hvi; Nets connected to LV nwell or nwell overlapping hvi but connected to LV voltages (i.e 1.8V) should be tagged "lv_net" using text.dg; This tag should be only on Li layer

Name	Description	Flags	Value	Unit
(hvnwell.8)	Min space between HV_nwell and any nwell on different nets		2.000	μm
(hvnwell.9)	(Nwell overlapping hvi) must be enclosed by hvi			
(hvnwell.10)	LVnwell and HnWell should not be on the same net (for the purposes of this check, short the connectivity through resistors); Exempt HnWell with li nets tagged "lv_net" using text.dg and Hnwell connected to nwell overlapping areaid.hl	TC		
(hvnwell.11)	Nwell connected to the nets mentioned in the "Power_Net_Hv" field of the latcup GUI must be enclosed by hvi (exempt nwell inside areaid.hl). Also for the purposes of this check, short the connectivity through resistors. The rule will be checked in the latchup run and exempted for cells "s8tsg5_tx_ibias_gen" and "s8bbcnv_psoc3p_top_18", "rainier_top, indus_top*", "rainier_top, manas_top, ccg3_top"			
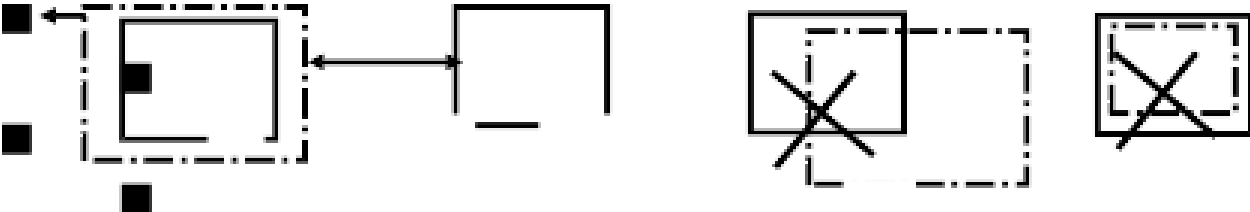
5.7.39 (hvdifftap.-)

Table 5.67: Function: Defines rules for HV diff/tap

Name	Description	Flags	Value	Unit
(hvd- iff- tap.14)	Min width of diff inside Hvi, except HV Pdiff resistors (difftap.14a)	P	0.290	µm
(hvd- iff- tap.14a)	Min width of diff inside Hvi, HV Pdiff resistors only	P	0.150	µm
(hvd- iff- tap.15a)	Min space of Hdiff to Hdiff	P	0.300	µm
(hvd- iff- tap.15b)	Min space of n+diff to non-abutting p+tap inside Hvi	P	0.370	µm
(hvd- iff- tap.16)	Min width tap butting diff on one or two sides inside Hvi (rule exempted inside UHVI)		0.700	µm
(hvd- iff- tap.17)	P+ Hdiff or Pdiff inside areaid:hvnwell must be enclosed by Hv_nwell by at least ….[Rule exempted inside UHVI]	DE NE	0.330	µm
(hvd- iff- tap.18)	Spacing of N+ diff to HV_nwell (rule exempted inside UHVI)	DE NE	0.430	µm
(hvd- iff- tap.19)	N+ Htap must be enclosed by Hv_nwell by at least …Rule exempted inside UHVI.	NE	0.330	µm
(hvd- iff- tap.20)	Spacing of P+ tap to HV_nwell (Exempted for p+tap butting pwell.rs; rule exempted inside UHVI)		0.430	µm
(hvd- iff- tap.21)	Diff or tap cannot straddle Hvi	P		
(hvd- iff- tap.22)	Min enclosure of Hdiff or Htap by Hvi. Rule exempted inside UHVI.	P	0.180	µm
(hvd- iff- tap.23)	Space between diff or tap outside Hvi and Hvi	P	0.180	µm
(hvd- iff- tap.24)	Spacing of nwell to N+ Hdiff (rule exempted inside UHVI)	DE NE	0.430	µm
(hvd- iff- tap.25)	Min space of N+ Hdiff inside HVI across non-abutting P+_tap	NC	1.070	µm
(hvd- iff- tap.26)	Min spacing between pwbm to difftap outside UHVI		N/A	N/A

5.7.40 (hvpoly.-)

Table 5.68: Function: Defines rules for HV poly

Name	Description	Flags	Value	Unit
(hvpoly.	Min width of poly over diff inside Hvi	P	0.500	µm
(hvpoly.	(poly and diff) cannot straddle Hvi			
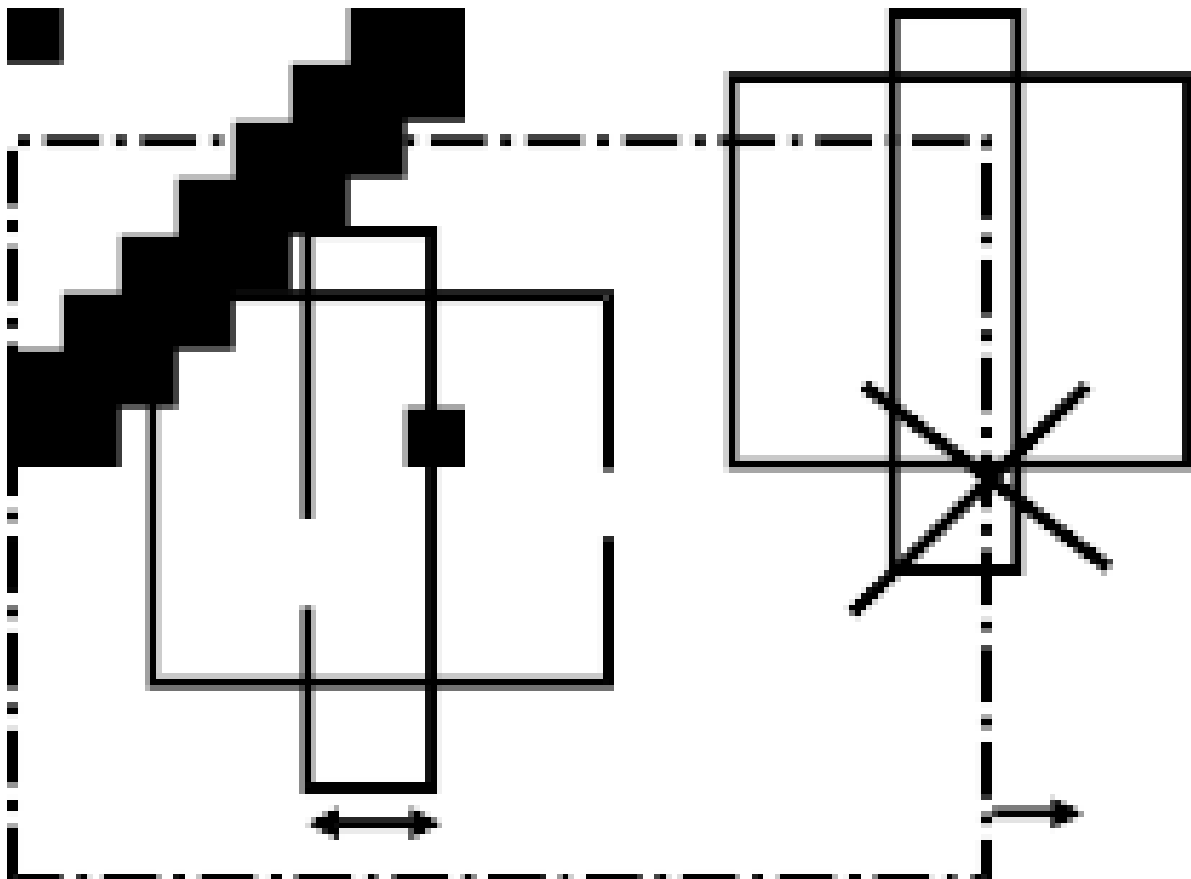
5.7.41 (hvntm.-)

Table 5.69: Function: Defines tip implants for the HV NMOS

Name	Description	Flags	Value	Unit
(hvntm.)	Hvntm can be drawn inside HVI. Drawn layer will be OR-ed with the CL and rechecked for CLDRC			
(hvntm.1	Width of hvntm	P	0.700	μm
(hvntm.2	Spacing of hvntm to hvntm	P	0.700	μm
(hvntm.3	Min. enclosure of (n+_diff inside Hvi) but not overlapping areaid.ce by hvntm	P	0.185	μm
(hvntm.4	Space, no overlap, between n+_diff outside Hvi and hvntm	P	0.185	μm
(hvntm.5	Space, no overlap, between p+_diff and hvntm	P DE	0.185	μm
(hvntm.6	Space, no overlap, between p+_tap and hvntm (except along the diff-butting edge)	P	0.185	μm
(hvntm.6	Space, no overlap, between p+_tap and hvntm along the diff-butting edge	P	0.000	μm
(hvntm.7	hvntm must enclose ESD_nwell_tap inside hvi by atleast	P	0.000	
(hvntm.9	Hvntm must not overlap areaid.ce			
(hvntm.1	Hvntm must overlap hvi			
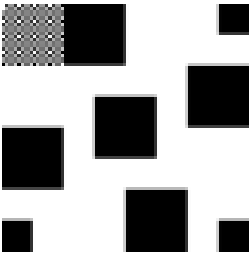
5.7.42 (denmos.-)

Table 5.70: Function: Defines rules for the 16V Drain extended NMOS devices

Name	Description	Flags	Value	Unit
(den-mos.1)	Min width of de_nFet_gate		1.055	μm
(den-mos.2)	Min width of de_nFet_source not overlapping poly		0.280	μm
(den-mos.3)	Min width of de_nFet_source overlapping poly		0.925	μm
(den-mos.4)	Min width of the de_nFet_drain		0.170	μm
(den-mos.5)	Min/Max extension of de_nFet_source over nwell		0.225	
(den-mos.6)	Min/Max spacing between de_nFet_drain and de_nFet_source		1.585	μm
(den-mos.7)	Min channel width for de_nFet_gate		5.000	μm
(den-mos.8)	90 degree angles are not permitted for nwell overlapping de_nFET_drain			
(den-mos.9a)	All bevels on nwell are 45 degree, 0.43 μm from corners	NC		μm
(den-mos.9b)	All bevels on de_nFet_drain are 45 degree, 0.05 μm from corners	NC		μm
(den-mos.10)	Min enclosure of de_nFet_drain by nwell		0.660	μm
(den-mos.11)	Min spacing between p+ tap and (nwell overlapping de_nFet_drain)		0.860	μm
(den-mos.12)	Min spacing between nwells overlapping de_nFET_drain		2.400	μm
(den-mos.13)	de_nFet_source must be enclosed by nsdm by		0.130	μm
(den-mos.14)	nvhv FETs must be enclosed by areaid.mt		N/A	N/A
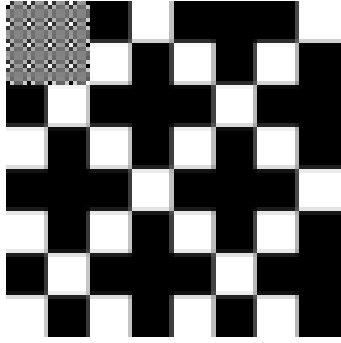
5.7.43 (depmos.-)

Table 5.71: Function: Defines rules for the 16V Drain extended NMOS devices

Name	Description	Flags	Value	Unit
(dep-mos.1)	Min width of de_pFet_gate		1.050	µm
(dep-mos.2)	Min width of de_pFet_source not overlapping poly		0.280	µm
(dep-mos.3)	Min width of de_pFet_source overlapping poly		0.920	µm
(dep-mos.4)	Min width of the de_pFet_drain		0.170	µm
(dep-mos.5)	Min/Max extension of de_pFet_source beyond nwell		0.260	
(dep-mos.6)	Min/Max spacing between de_pFet_drain and de_pFet_source		1.190	µm
(dep-mos.7)	Min channel width for de_pFet_gate		5.000	µm
(dep-mos.8)	90 degree angles are not permitted for nwell hole overlapping de_pFET_drain			
(dep-mos.9a)	All bevels on nwell hole are 45 degree, 0.43 µm from corners	NC		µm
(dep-mos.9b)	All bevels on de_pFet_drain are 45 degree, 0.05 µm from corners	NC		µm
(dep-mos.10)	Min enclosure of de_pFet_drain by nwell hole		0.860	µm
(dep-mos.11)	Min spacing between n+ tap and (nwell hole enclosing de_pFET_drain)		0.660	µm
(dep-mos.12)	de_pFet_source must be enclosed by psdm by		0.130	µm
(dep-mos.13)	pvhv fets(except those with W/L = 5.0/0.66) must be enclosed by areaid.mt		N/A	N/A
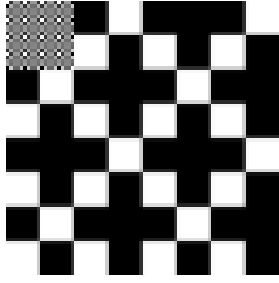
5.7.44 (extd.-)

Table 5.72: Function: Defines rules areaid.en

Name	Description	Flags	Value	Unit
(extd.1)	Difftap cannot straddle areaid:en			
(extd.2)	DiffTap must have 2 or 3 coincident edges with areaid:en if enclosed by areaid:en			
(extd.3)	Poly must not be entirely overlapping difftap in areaid:en			
(extd.4)	Only cell name "s8rf_n20vhv1*" is a valid cell name for n20vhv1 device (Check in LVS as invalid device)		N/A	N/A
(extd.5)	Only cell name "s8rf_n20vhviso1" is a valid cell name for n20vhviso1 device (Check in LVS as invalid device)		N/A	N/A
(extd.6)	Only cell name "s8rf_p20vhv1" is a valid cell name for p20vhv1 device (Check in LVS as invalid device)		N/A	N/A
(extd.7)	Only cell name "s8rf_n20nativevhv1*" is a valid cell name for n20nativevhv1 device (Check in LVS as invalid device)		N/A	N/A
(extd.8)	Only cell name "s8rf_n20zvtvhv1*" is a valid cell name for n20zvtvhv1 device (Check in LVS as invalid device)		N/A	N/A
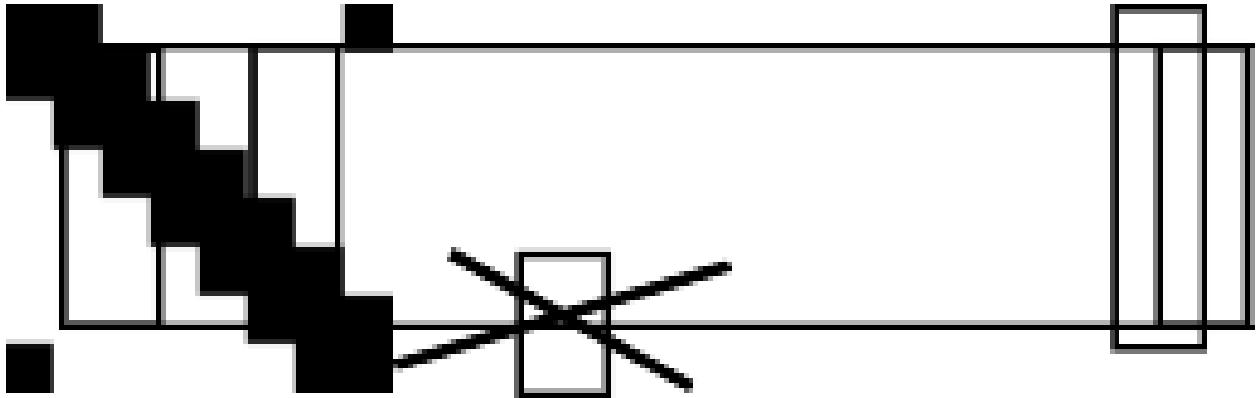
5.7.45 (hv.-.-)

Note: High voltage rule apply for an operating voltage range of 5.5 - 12V; Nodes switching between 0 to 5.5V do not need to follow these rules

Table 5.73: Function: Defines High Voltage Rules (FIXME)

Name	Description	Flags	Value	Unit
(hv.X.1)	High voltage source/drain regions must be tagged by diff:hv			
(hv.X.3)	High voltage poly can be drawn over multiple diff regions that are ALL reverse-biased by at least 300 mV (existence of reverse-bias is not checked by the CAD flow). It can also be drawn over multiple diffs when all sources and all drain are shorted together. In these case, the high voltage poly can be tagged with the text:dg label with a value "hv_bb". Exceptions to this use of the hv_bb label must be approved by technology. Under certain bias conditions, high voltage poly tagged with hv_bb can cross an nwell boundary. The poly of the drain extended device crosses nwell by construction and can be tagged with the "hv_bb" label. Use of the hv_bb label on high voltage poly crossing an nwell boundary must be approved by technology. All high voltage poly tagged with hv_bb will not be checked to hv.poly.1, hv.poly.2, hv.poly.3 and hv.poly.4.			
(hv.X.4)	Any piece of layout that is shorted to hv_source/drain becomes a high voltage feature.			
(hv.X.5)	In cases where an hv poly gate abuts only low voltage source and drain, the poly gate can be tagged with the text:dg label with a value "hv_lv". In this case, the "hv_lv" tagged poly gate and its extensions will not be checked to hv.poly.6, but is checked by rules in the poly.-.- section. The use of the hv_lv label must be approved by technology.			
(hv.X.6)	Nwell biased at voltages >= 7.2V must be tagged with text "shv_nwell"	NC		
(hv.nwel	Min spacing of nwell tagged with text "shv_nwell" to any nwell on different nets		2.500	μm
(hv.diff.1	Minimum hv_source/drain spacing to diff for edges of hv_source/drain and diff not butting tap		0.300	μm
(hv.diff.1	Minimum spacing of (n+/p+ diff resistors and diodes) connected to hv_source/drain to diff		0.300	μm
(hv.diff.2	Minimum spacing of nwell connected to hv_source/drain to n+ diff	DE	0.430	μm
(hv.diff.3	Minimum n+ hv_source/drain spacing to nwell		0.550	μm
(hv.diff.3	Minimum spacing of (n+ diff resistors and diodes) connected to hv_source/drain to nwell		0.550	μm
(hv.poly.	Hv poly feature hvPoly (including hv poly resistors) can be drawn over only one diff region and is not allowed to cross nwell boundary except (1) as allowed in rule .X.3 and (2) nwell hole boundary in depmos			
(hv.poly.	Min spacing of hvPoly (including hv poly resistor) on field to diff (diff butting hvPoly are excluded)		0.300	μm
(hv.poly.	Min spacing of hvPoly (including hv poly resistor) on field to n-well (exempt poly straddling nwell in a denmos/depmos)		0.550	μm
(hv.poly.	Enclosure of hvPoly (including hv poly resistor) on field by n-well (exempt poly straddling nwell in a denmos/depmos)		0.300	μm
(hv.poly.	Min extension of poly beyond hvFET_gate (exempt poly extending beyond diff along the S/D direction in a denmos/depmos)		0.160	
(hv.poly.	Extension of hv poly beyond FET_gate (including hvFET_gate; exempt poly extending beyond diff along the S/D direction in a denmos/depmos)		0.160	
(hv.poly.	Minimum overlap of hv poly ring_FET and diff			
(hv.poly.	Any poly gate abutting hv_source/drain becomes a hvFET_gate			

5.7.46 (vhvi.-.-)

Table 5.74: Function: Identify nets working between 12-16V

Name	Description	Flags	Value	Unit
(vhvi.vhv	Terminals operating at nominal 12V (maximum 16V) bias must be tagged as Very-High-Voltage (VHV) using vhvi:dg layer	NC		
(vhvi.vhv	A source or drain of a drain-extended device can be tagged by vhvi:dg. A device with either source or drain (not both) tagged with vhvi:dg serves as a VHV propagation stopper	NC		
(vhvi.vhv	Any feature connected to VHVSourceDrain becomes a very-high-voltage feature	NC		
(vhvi.vhv	Any feature connected to VHVPoly becomes a very-high-voltage feature	NC		
(vhvi.vhv	Diffusion that is not a part of a drain-extended device (i.e., diff not areaid:en) must not be on the same net as VHVSourceDrain. Only diffusion inside areaid.ed and LV diffusion tagged with vhvi:dg are exempted.			
(vhvi.vhv	Poly resistor can act as a VHV propagation stopper. For this, it should be tagged with text "vhv_block"	NC		
(vhvi.1.-)	Min width of vhvi:dg		0.020	µm
(vhvi.2.-)	Vhvi:dg cannot overlap areaid:ce			
(vhvi.3.-)	VHVGate must overlap hvi:dg			
(vhvi.4.-)	Poly connected to the same net as a VHVSourceDrain must be tagged with vhvi:dg layer			
(vhvi.5.-)	Vhvi:dg cannot straddle VHVSourceDrain			
(vhvi.6.-)	Vhvi:dg overlapping VHVSourceDrain must not overlap poly			
(vhvi.7.-)	Vhvi:dg cannot straddle VHVPoly			
(vhvi.8.-)	Min space between nwell tagged with vhvi:dg and deep nwell, nwell, or n+diff on a separate net (except for n+diff overlapping nwell tagged with vhvi:dg).		11.24	µm

5.7.47 (uhvi.-.-)

Table 5.75: Function: Identify nets working between 20V

Name	Description	Flags	Value	Unit
(uhvi.1.-)	diff/tap can not straddle UHVI		N/A	N/A
(uhvi.2.-)	poly can not straddle UHVI		N/A	N/A
(uhvi.3.-)	pwbm.dg must be enclosed by UHVI (exempt inside areaid.lw)		N/A	N/A
(uhvi.4.-)	dnw.dg can not straddle UHVI		N/A	N/A
(uhvi.5.-)	UHVI must enclose areaid.ext		N/A	N/A
(uhvi.6.-)	UHVI must enclose dnwell		N/A	N/A
(uhvi.7.-)	natfet.dg must be enclosed by UHVI layer by at least		N/A	N/A
(uhvi.8.-)	Minimum width of natfet.dg		N/A	N/A
(uhvi.9.-)	Minimum Space spacing of natfet.dg		N/A	N/A
(uhvi.10)	natfet.dg layer is not allowed		N/A	N/A

5.7.48 (ulvt-.-)

Table 5.76: Function: Identify dnwdiodehv_Psub(BV~60V)

Name	Description	Flags	Value	Unit
(ulvt-.1)	areaid.low_vt must enclose dnw for the UHV dnw-psub diode texted "condiodeHvPsub"		NA	
(ulvt-.2)	areaid.low_vt must enclose pwbm.dg for the UHV dnw-psub diode texted "condiodeHvPsub"		NA	
(ulvt-.3)	areaid.low_vt can not straddle UHVI		NA	

5.7.49 (pwres.-.-)

Table 5.77: Function: Identify pwell resistors

Name	Description	Flags	Value	Unit
(pwres.1)	Pwell resistor has to be enclosed by the res layer	NC		
(pwres.2)	Min/Max width of pwell resistor		2.650	µm
(pwres.3)	Min length of pwell resistor		26.50	µm
(pwres.4)	Max length of pwell resistor		265.0	µm
(pwres.5)	Min/Max spacing of tap inside the pwell resistor to nwell		0.220	µm
(pwres.6)	Min/Max width of tap inside the pwell resistor		0.530	µm
(pwres.7)	Every pwres_terminal must enclose 12 licon1			
(pwres.7)	Every pwres_terminal must enclose 12 mcons if routed through metal1			
(pwres.8)	Diff or poly is not allowed in the pwell resistor.			
(pwres.9)	Nwell surrounding the pwell resistor must have a full ring of contacted tap strapped with metal.			
(pwres.1)	The res layer must abut pwres_terminal on opposite and parallel edges			
(pwres.1)	The res layer must abut nwell on opposite and parallel edges not checked in Rule pwres.10			

5.7.50 (rfdiode.-.-)

Table 5.78: Function: Identify RF diodes; Used for RCX

Name	Description	Flags	Value	Unit
(rfdiode.)	Only 90 degrees allowed for areaid.re			
(rfdiode.)	areaid.re must be coincident with nwell for the rf nwell diode			
(rfdiode.)	areaid.re must be coincident with innwer edge of the nwell ring for the rf pwell-deep nwell diode Allowed PNP layout Layout: pnppar Allowed NPN layout Layout: npnpar1x1			
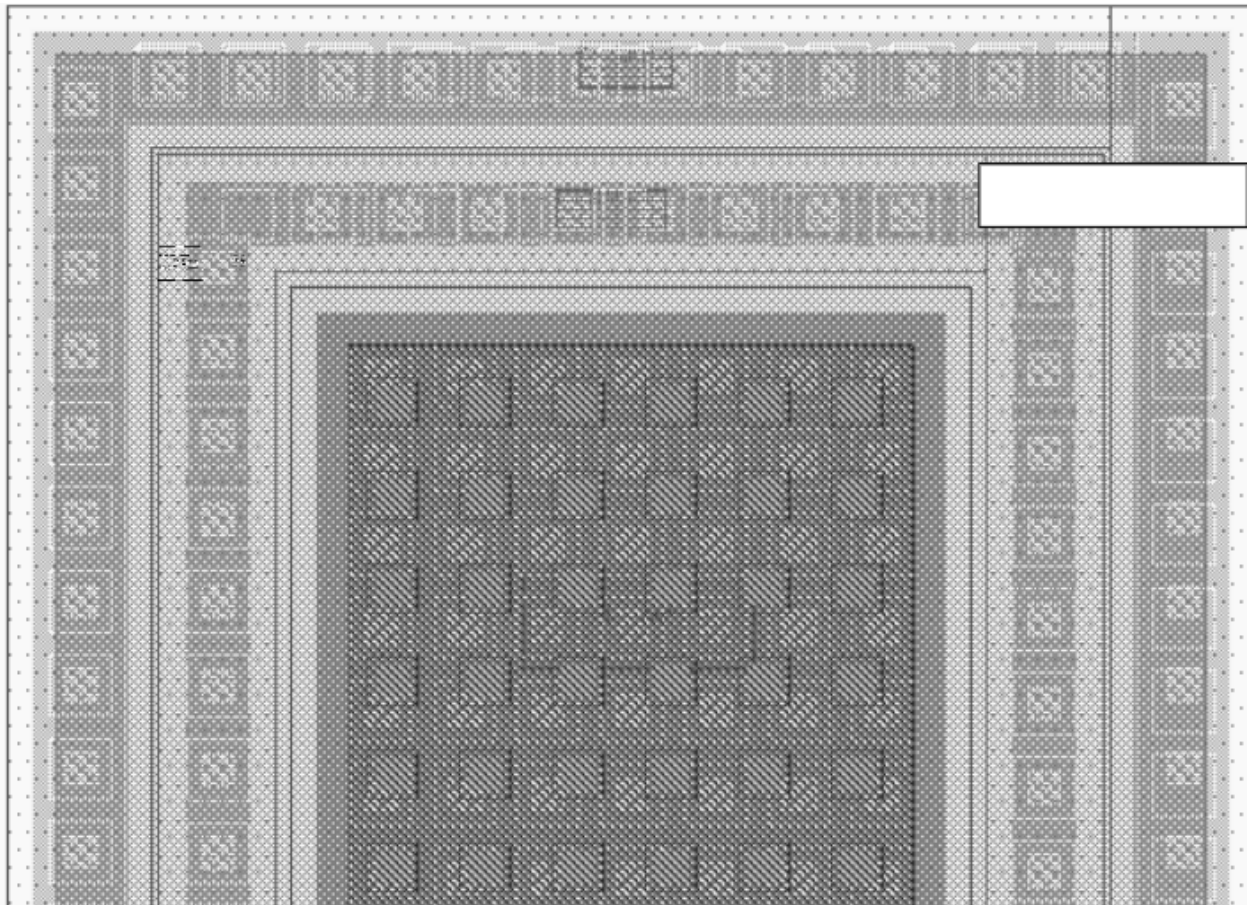
5.8 WLCSP Rules

Table 5.79: Amkor WLCSP

Allowed pitch		Supported flows		Al
400 um	500 um	s8p-5rns8p-10r*ns8pf-10r*ns8pfn-20r*ns8p12-10r*ns8spf-10r*		40
(pi1.-.-)	(pi1_500.-.-)	1st polyimide layer for WLCSP		
		Function: Opens over the pad openings; Allows RDL layer to connect to top metal		
1	1	Min width of pi1 (for parallel opposite edges)		35
2	2	Min spacing between pi1		20
3	3	pi1 must be enclosed by pad by atleast		7.
(rdl.-)	(rdl_500.-)	Re-distribution layer		
		Function: Re-distribution layer connects the top metal from the customer to the bumps		
1	1	Min width of rdl (for parallel opposite edges)		10
2	2	min spacing between two rdl		10
3	3	pi1 must be enclosed by rdl by atleast		10
(pi2.-.-)	(pi2_500.-.-)	2nd polyimide layer for WLCSP		
		Function: 2nd polyimide layer acts as a via between RDL and UBM		
1	1	Min width of pi2 (for parallel opposite edges)		17
3	3	Min spacing, no overlap, between pi1 and pi2		25
(ubm.-.-)	(ubm_500.-.-)	Under bump metal		
		Function: Layer added underneath the bump balls		
1	1	Min width of ubm (for parallel opposite edges)		21
3	3	pi2 must be enclosed by ubm by atleast		15
4	4	ubm must be enclosed by rdl by atleast		10
5	5	Min spacing, no overlap, between pi1 and ubm		10
6	6	Min spacing between center of ubm and outer edge of the seal ring		15
(bump.-.-)	(bump_500.-.-)	Bump balls for WLCSP		
		Function: WLCSP bump balls		
1	1	Min width of bump (for parallel opposite edges)		26
2	2	Min/Max pitch spacing between bump (center to center)		40
2a	2a	Min/Max pitch spacing between bump (center to center) across the scribe	NC	40
3	3	Min spacing between bump and outer edge of the seal ring		25
4	4	Min size of Chip_extent overlapping bump.dg		75
5	5	Max size of Chip_extent overlapping bump.dg		68

(cpbo.-.-)	1st polyimide (mask)
	Function: Opens over the pad openings; Allows RDL layer to connect to top metal
wlcsp.1	Min cpbo diameter over bond pad passivation opening
wlcsp.2	Min bond pad passivation opening to create cpbo
wlcsp.3	Min enclosure of cpbo over bond pad by pad:dg
(rdl.-)	Re-distribution
	Function: Re-distribution layer connects the top metal from the customer to the bumps
x.1	Polymer 1 via and RDL1 capture pad should be designed as large as possible. The shape can be a circle, octagon, oblo
x.2	Fillet or "teardrop" is required between the trace and the RDL1 UBM capture pad to reduce stress and avoid 90°or acu
x.3	Trace width and spacing shall be made equal and maximized where possible for optimized manufacturability, reliabilit
wlcsp.1	Min rdl pad diameter over bond pad
wlcsp.2	Min spacing between rdl and rdl larger than 30 um by 30 um and a run length > 60um
wlcsp.3	cpbo (with max width of 30x30 must be enclosed by rdl by at least

(cpbo.-.-)	1st polyimide (mask)
(cpmm2.-.-)	2nd polyimide
	Function: 2nd polyimide layer acts as a via between RDL and UBM
x.1	Capture pads are identified by (rdl and bump) enclosing pmm2
wlcsp.1	Min spacing, no overlap, between cpbo and cpi2 on different nets
wlcsp.2	Min enclosure of cpbo by cpmm2 (no straddle)
wlcsp.3	Min cpmm2 pad diameter
wlcsp.4	Min diameter of rdl capture pad under cpmm2
wlcsp.5	Min enclosure of rdl by cpmm2
wlcsp.6	Minimum remaining fraction (polymer 2) size of full via sizenAdd a radius or chamfer on sharp corners of truncated 2
(ubm.-.-)	Under bump metal
	Function: Layer added underneath the bump balls
1	Min width of ubm (for parallel opposite edges)
2	pmm2 must be enclosed by ubm by atleast
3	Min spacing between center of ubm and outer edge of the seal ring
(bump.-.-)	Bump balls for WLCSP
	Function: WLCSP bump balls
1	Min width of bump (for parallel opposite edges)
2	Min/Max pitch spacing between bump (center to center w/2x snapGrid tolerance)

5.9 High Voltage Methodology

High Voltage is defined as a voltage outside the range of GND to Vcc. Any device that is subjected to a voltage outside the range of GND to Vcc is considered a high voltage device. These devices are subjected to special design rules and biasing conditions. The biasing conditions of these high voltage devices are detailed in the ETD.

5.9.1 Failure Mechanisms in High Voltage Devices

The TDR have a special rules section for the layout and DRC of the high voltage (hv) device.

These rules are framed so as to prevent the following failure mechanisms in circuits that use these devices:

Transistor Performance Degradation under HV Gate Stress (Section 2.2.2 of EDR)
  The maximum voltage across the gate oxide (gate to channel voltage) is restricted to:

  a. Any HV NMOS device: 7.3 V @ 25C.

  b. Any HV PMOS device: 8.1 V @ 25C.

  These voltages are not operating voltages, but points of failure. They should not be exceeded in any circuit at any time.

Junction Leakage/breakdown
  The maximum source/drain to substrate junction voltages are restricted to the following:

  a. Any HV NMOS device: 11.0 V @ 25C.

  b. Any HV PMOS device: 11.0 V @ 25C.

  These voltages are not operating voltages, but points of failure. They should not be exceeded in any circuit at any time.

Gated-Diode Leakage/Breakdown
  All high voltage devices use 110A gate oxide thickness just like low voltage (0 to Vcc) devices.

The maximum gate-to-junction voltage differentials should be not exceed the voltage criteria set by conditions (1) and (2) above.

In addition, hv p-channel devices are required to be laid out as ring devices (also called half-fieldless and fieldless devices), where the hv junction does not abut field oxide edge. These devices also get the extra junction grading implant into the ringed gate with the HVPDM mask.

Source to Drain Punch-through

To prevent punch-through, the hv devices have expanded channel lengths:

    a. HV NMOS/PMOS device channel length = 0.500 um final.

Parasitic Isolation Field Leakage

HV poly is prohibited from forming gates with adjacent hv diffusions, and from crossing well boundaries.

Exceptions to this rule are made only in cases where the bulk of the isolation device formed is back-biased by at least 300 mV.

The presence of the back bias cannot be checked by the CAD flow at this time. Exceptions pass clean through DRC with the presence of the "hv_bb" tag on the hv poly.

The usage of the hv_bb tag is subject to approval by technology.

Sub-threshold EndCap Leakage

The extension of poly forming a high voltage gate onto field to prevent subthreshold leakage due to line-end shortening of the poly/field oxide endcap.

5.9.2 High Voltage Implementation Methodology

Following are the features of the high voltage rules:

High Voltage Diffusion (hvSRCDRN)

The source of high voltage is a diffusion(source/drain) tagged within the high voltage identification layer diff:hv. The whole diffusion feature need to be completely enclosed by the diff:hv layer.

The source/drains that are tagged with the diff:hv layer are called taggedhvSRCDRN within the CAD flow code. The propagation of the high voltage property within the tagged piece of diffusion stops at a gate, i.e.. if tagging is done on the drain side, the source does not become a high voltage feature.

Beginning with taggedhvSRCDRN, high voltage propagates through standard interconnect to other SRCDRN or poly. Any SRCDRN derives the high voltage property through electrically shorting to a taggedhvSRCDRN is called a derivedhvSRCDRN within the CAD flow. Hence by definition, within the CAD flow,

    hvSRCDRN = OR(taggedhvSRCDRN derivedhvSRCDRN)

Rule hv.X.1 (high voltage source/drain regions must be tagged by diff:hv) will check the presence of the diff:hv tag and flag on all derivedhvSRCDRN. When the layout is finally clean of all hv.diff.1 errors, hvSRCDRN will consist of only taggedhvSRCDRN (all derivedhvSRCDRN will need to be tagged with diff:hv to remove errors). This is shown in Fig.1.

Rule hv.diff.1 (Minimum hv_source/drain spacing to diff for edges of hv_source/drain and diff not butting tap) prevents adjacent diffusions from punching through. Note that this rule specifies the spacing of a hvSRCDRN to any diffusion – be it another hvSRCDRN or a normal diffusion. This rule also applies to N+/P+ resistors that become hv by propagation. This is shown schematically in Fig.2.

Rule hv.diff.2 (P-channel hv_source/drain must be enclosed by a ring_FET gate) is required to prevent excess field oxide/gate edge leakage in high voltage p-channel devices (Fig.3). This ring_FET gate by definition is a hvring_FET (as it abuts hv diff).

High Voltage Poly (hvPoly)

A high voltage poly feature (hvPoly) is defined as a poly feature which is electrically shorted to hvSRCDRN, or

to another high voltage feature (like another hvPoly) through an interconnect. The whole poly feature becomes high voltage feature.

hvpoly propagates the high voltage property to other features which are electrically shorted (through licon1 & li1); but does not act as a source of high voltage. This means that hvpoly does not make underlying diffusions or wells high voltage – it acts as a "conductor" and propagates the high voltage property to other electrically connected features.

hvpoly cannot form parasitic field isolation devices, unless this device is back-biased. Hence, the following rules are in place:

`hv.poly.1`

> Hv poly feature can be drawn over only one diff region and is not allowed to cross nwell boundary except as allowed in rule hv.X.3. Please refer to Fig.4.

`hv.X.3`

> High voltage poly can be drawn over multiple diff regions that are ALL reverse-biased by at least 300 mV (existence of reverse-bias is not checked by the CAD flow).
>
> In this case, the high voltage poly can be tagged with the `text:dg` label with a value "hv_bb".
>
> Exceptions to this use of the hv_bb label must be approved by technology.
>
> Under certain bias conditions, high voltage poly tagged with hv_bb can cross an nwell boundary.
>
> Use of the hv_bb label on high voltage poly crossing an nwell boundary must be approved by technology.
>
> This is shown in Fig.5.
>
> All high voltage poly tagged with hv_bb will not be checked to `hv.poly.1`, `hv.poly.2`, `hv.poly.3` and `hv.poly.4`.
>
> - `hv.poly.2`: Spacing of hv poly on field to unrelated diff (Fig.6).
> - `hv.poly.3`: Spacing of hv poly on field to n-well (Fig.6).
> - `hv.poly.4`: Enclosure of hv poly on field by n-well (Fig.6).

Poly resistors can become high voltage features if the poly is electrically shorted to hvSRCDRN, or to another high voltage feature. Nevertheless, these devices cannot act as sources of hv, and the hv propagation stops at the edge of this device.

High Voltage Poly Gate (hvFET_gate)

> A high voltage poly gate (`hvFET_gate`) is a gate (`PolyAndDiff`) abutting hvSRCDRN. This is specified in rule `hv.poly.8` (Any poly gate abutting hv_source/drain becomes a high voltage poly gate).
>
> Note that this is the only definition of a hvFET_gate and the only way a gate can become a hvFET_gate.
>
> This is shown schematically in Fig.7.
>
> The high voltage property of the `hvFET_gate` is limited to the gate only – the whole poly feature does not become a hvPoly.
>
> The following rules are in place for hvFET_gates (please refer to Fig.12):
>
> - `hv.diff.2`: P-channel hv_source/drains must be enclosed by a ring_FET gate. This is required to prevent excess field oxide/gate edge leakage in high voltage p-channel devices. A p-channel hvring_FET gate is shown schematically in Fig.8.
> - `hv.poly.5`: Hv poly gate length (which is bigger than a normal gate length)
> - `hv.poly.6`: Extension of poly forming an `hvFET_gate` beyond hv diffusion
> - `hv.poly.7`: Minimum overlap of poly forming `hvring_FET` and diffusion

Stoppers to High Voltage Propagation

The following act as stoppers for hv propagation (shown in Fig.10):

- For a `hv_source/drain` tagged with `diff:hv`, the high voltage property terminates at the intersection of this hv diff with a poly, i.e. at the gate edge. This means that one side of the device can have a hv diff, while the other side of the gate can remain low voltage.

- N+/P+ diffusion resistors are allowed per the Allowed Resistors table in the TDR. These resistors do not originate high voltage. They also do not propagate high voltage, although the device itself becomes a high voltage device. The hv rule hv.diff.1 needs to be checked for these devices.

- Diodes do not originate high voltage. Nevertheless, they propagate high voltage and become high voltage devices when high voltage is propagated to them. The hv rule hv.diff.1 needs to be checked for these devices.

- A poly forming a poly resistor can become hvPoly by virtue of shorting to a hv_source/drain or shorting to another high voltage feature through an interconnect. The high voltage propagation stops at a poly resistor, although the device itself becomes high voltage. This device will be checked to the following hv rules: hv.poly.1, hv.poly.2, hv.poly.3, and hv.poly.4. These rule checks can be exempted by the use of the "hv_bb" tag with the approval of technology.

- The high voltage propagation also stops at a P-Well resistor. The device becomes a hv device. There are no specific rule checks for this hv device.

Summary of High Voltage Propagation

The high voltage propagation methodology is summarized below in Table 1.

A test case utilizing the outlined methodology is shown in Fig.12.

Table 5.81: Table 1. Truth table for high voltage generation, propagation and retention.

Node Type	Originates HV?	Propa-gates HV?	Becomes HV? (when HV Propagates to this node)	Notes
Deep N-Well	No	N/A	N/A	17
P-Well	No	N/A	N/A	Page 139, 1Page 139, 7
P-Well Resistor	No	No	Yes	2
N-Well	No	N/A	N/A	Page 139, 1Page 139, 7
waffle_chip	No	Yes	Yes	
P+ Diffusion	No	Yes	Yes	
N+ Diffusion Resistor	No	No	Yes	3
P+ Diffusion Resistor	No	No	Yes	Page 139, 3
HV Diffusion	Yes	Yes	Yes	
Diodes	No	Yes	Yes	Page 139, 3
Poly	No	Yes	Yes	
Poly Resistor	No	No	Yes	4
GATE	No	No	No	
HvFET_gate (GATE abutting hv Diff)	No	No	Yes	5
Licon1	No	Yes	N/A	6
Li1	No	Yes	N/A	Page 139, 6
Mcon	No	Yes	N/A	Page 139, 6
Met1	No	Yes	N/A	Page 139, 6
Via	No	Yes	N/A	Page 139, 6
Met2	No	Yes	N/A	Page 139, 6

5.10 Very High Voltage Methodology

Very High Voltage is defined as a voltage outside the range of GND to High Voltage (11V). Very high voltage is 16V (12V nominal) Vcc.

Any device that is subjected to a voltage outside the range of GND to 11V is considered a Very High Voltage (VHV) device.

These devices are subjected to special design rules and biasing conditions.

5.10.1 Failure Mechanisms in VHV Devices

The TDR have a special rules section for the layout and DRC of the VHV device.

These rules are framed so as to prevent the following failure mechanisms in circuits that use these devices:

Transistor Performance Degradation under VHV Gate Stress

The maximum voltage across the gate oxide (gate to channel voltage) is restricted to:

a. Any VHV NMOS device: 5.5V.

b. Any VHV PMOS device: 5.5V.

Junction Leakage/breakdown

The maximum source/drain to substrate junction voltages are restricted to the following:

a. Any VHV NMOS device: 16.0V.

b. Any VHV PMOS device: 16.0V.

Gated-Diode Leakage/Breakdown:

All VHV devices use 110A gate oxide thickness just like standard 5.0V Vcc devices.

The maximum gate-to-junction voltage differentials should not exceed the voltage criteria set by conditions (1) and (2) above.

The VHV devices need to be designed with drain extentions (DE) fabricated by lightly doped Nwells and Pwell-srespectively. Under no circumstances the poly/extended drain overlap and field oxide length should be changed.

Source to Drain Punch-through

To prevent punch-through, the VHV devices have expanded channel lengths:

a. VHV NMOS device channel length = 1.055 um drawn.

b. VHV PMOS device channel length = 1.050 um drawn.

Parasitic Isolation Field Leakage

Poly from a drain extended device is prohibited from forming gates with adjacent hv diffusions.

Sub-threshold EndCap Leakage

The extension of poly forming a high voltage gate onto field to prevent subthreshold leakage due to line-end shortening of the poly/field oxide endcap.

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[1] Deep N-Wells, N-Wells and P-Wells cannot be used as routing layers.

[7] "N/A" implies that there are no special hv rules for these layers.

[2] No hv rule checks for this device.

[3] For N+ and P+ diffusion resistors and diodes, rule hv.diff.1 (spacing to unrelated diff) needs to be checked.

[4] Need to be checked for hv.poly.1, hv.poly.2, hv.poly.3, hv.poly.4. Needs technology approval for use of hv.X.3.

[5] The hv property is localized to the hvgate and its extensions.

[6] Interconnect and contacts propagate hv, and are hv devices internal to the CAD flow only.

Reliability performance:

In order to preserve the reliability performance of the VHV FETs the Field Oxide (STI) length may not be changed from the values below:

a. VHV NMOS STI length = 1.585 um

b. VHV PMOS STI length = 1.190 um

A poly gate may never be directly connected to a VHV diffusion region.

Poly connecting two VHV nodes over field must be routed through LI or metal.

5.10.2 VHV Implementation Methodology

Following are the features of the VHV rules:

- All features operating at 16V (max) voltages can be Very-High-Voltage (VHV)

- Drain or source of the drain-extended device can be tagged with vhvi:dg layer. Device with either drain or source (not both) tagged with vhvi:dg layer serves as propagation stopper

- The VHVSourceDrain can be connected to another VHVSourceDrain or an output pad. The VHVSourceDrain does not propagate the VHV through the device

- All source/drains/gate tagged with vhvi:dg propagate VHV through any interconnects.

- Diff inside areaid.ed on the same net as VHVSourceDrain should be tagged with vhvi:dg. They serve as propagation stopper.

- Deep N-well, N-well, P-well, Diff, or Poly cannot be used as routing layers.

Table 5.82: Table 2 - Truth table for very high voltage generation, propagation and retention.

Node Type	Originates VHV?	Propagates VHV?	Requires tagging with vhvi:dg (flags if not tagged when required)
Deep N-Well	No	N/A	N/A
P-Well	No	N/A	N/A
P-Well Resistor	No	No[8]	Yes
N-Well	No	N/A	N/A
LV Diffusion	No	Yes	Yes
Diffusion Resistor	No	No[Page 141, 8]	Yes
HV Diffusion	No	Yes	Yes
VHV ESD Diffusion	No	No	Yes
VHV-SourceDrain	Yes	No[9]	Yes
Diodes	No	Yes	Yes
Poly	No	N/A	N/A
Poly Resistor	No	No[8]	Yes
VHVPoly	Yes	Yes	Yes
GATE	No	N/A	N/A
de_pFET_gate	No	N/A	N/A
de_nFET_gate	No	N/A	N/A
Licon1	No	Yes	No
Li1	No	Yes	No
Mcon	No	Yes	No
Met1	No	Yes	No
Via	No	Yes	No
Met2	No	Yes	No
via2	No	Yes	No
Met3	No	Yes	No

5.11 Antenna Rules

Antenna rules specify the maximum allowed ratio of interconnect area exposed to plasma etch to active gate poly area that is electrically connected to it when the interconnect is etched. Interconnect areas exposed to plasma etch are:

- bottom areas of Licon, Mcon, Via, Via2

- perimeter areas of connection layers Poly, Li, Met1, Met2, Met3

Two types of checks are introduced in the following tables:

- vertical for perimeter area, and

- horizontal for contact area

The numbers checked for are in the MAX_EGAR column.

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[8] Resistors tagged with text "''vhv_block''" serve as VHV propagation stopper and it is the duty of the designer to ensure that the resistor can support the required voltage drop. Otherwise components in VHV nets need to be tagged with vhvi:dg layer

[9] If only source or drain is tagged with vhvi:dg layers.

5.11.1 Definitions

Table 5.83: Antenna Rules Definitions

Symbol	Explanation	Unit
PI	Perimeter of Interconnect	um
FLT	Final Layer thickness	um
W	Width of MOS Transistor	um
L	Length of MOS Transistor	um
A	Area of MOS Transistor gate (= W x L)	um2
CA	Area of contact or via	um2
SW	Sidewall area (= PI x FLT)	um2
EA	Etched area (= CA for horizontal, = SW for vertical areas)	um2

Antenna rule numbers depend on the connection to the following devices:

pAntennaShort = (tap AndNot poly) AndNot nwell

It is a p+ tap contact used to shortcut to substrate ground buses.

AntennaDiode = (diff OR tap) AndNot (poly OR pAntennaShort)

It is a reverse biased diode whose leakage current will discharge the interconnect area.

These devices are not subject to LVS check and must not be reported in the schematic.

Antenna rules are defined for the following ratio:

When a diode is used

EGAR

Etch Gate Area Ratio = (EA / A_gate) - K x (AntennaDiode_area in um2) - diode_bonus [unitless]

When diodes are not used

EGAR

Etch Gate Area Ratio = (EA / A_gate) [unitless]

where:

- K is a multiplying factor specified for each layer

- AntennaDiode_area is the area of the AntennaDiode used to discharge the interconnect area exposed to plasma etch (should be 0 if no diode is used)

The layout should satisfy the condition: EGAR <= MAX_EGAR. The diode_bonus applies only when at least one diode is used, regardless from it's size.

5.11.2 Tables

Todo: Most of these tables should be removed.

Table 5.84: Table Ia. Antenna rules (S8D*)

	Antenna ratios	Area checked: H/V	FLT	MAX_EGA		
(ar_q.-.-)				Max EA/A w/o diode	K	Diode bonus
.poly.1	Poly (poly perimeter area/gate area)	Vertical	0.180	50	n/a	n/a
.licon.1	Licon (licon1 area/gate area)	Horizontal		3	n/a	n/a
.li.1	LI (LI perimeter area/gate area)	Vertical	0.100	75	450	n/a
.mcon.1	Mcon (mcon area/gate area)	Horizontal		3	18	n/a
.met1.1	Met1 (met1 perimeter area/gate area)	Vertical	0.350	400	400	2200
.via.1	Via (via area/gate area)	Horizontal		6	36	n/a
.met2.1	Met2 (met2 perimeter area/gate area)	Vertical	0.350	400	400	2200
.pad.1	pad (via2 area/gate area)	Horizontal		6	36	n/a
.indm.1	INDM (met3 perimeter area/gate area)	Vertical	4.000	400	400	2200
.ar.1	Antenna rules not checked for features connected to a pAntennaShort					
Design limitations due to antenna rules (FET gate = 1um2).		w/o diode		with 1um2 diode		
Max length of Poly (approx, assumes min width)		135		n/a		
Max number of Licons		103		n/a		
Max length of LI (approx, assumes min width)		370		2620		
Max number of Mcon		103		726		
Max length of Met1 (approx, assumes min width)		570		4280		
Max number of Via		266		1866		
Max length of Met2 (approx, assumes min width)		570		4280		
Max number of pad via		4		29		
Max length of Met3 (approx, assumes min width)		45		370		

Table 5.85: Table Ib. Antenna rules (S8TNV-5R)

Table Ib. Antenna rules (S8TNV-5R)		Antenna ratios	Area checked: H/V	FLT	MAX_EGA		
(ar_q.-.-)					Max EA/A w/o diode	K	Diode bonus
.poly.1		Poly (poly perimeter area/gate area)	Vertical	0.180	50	n/a	n/a
.licon.1		Licon (licon1 area/gate area)	Horizontal		3	n/a	n/a
.li.1		LI (LI perimeter area/gate area)	Vertical	0.100	75	450	n/a
.mcon.1		Mcon (mcon area/gate area)	Horizontal		3	18	n/a
.met1.1		Met1 (met1 perimeter area/gate area)	Vertical	0.350	400	400	2200
.via.1		Via (via area/gate area)	Horizontal		6	36	n/a
.met2.1		Met2 (met2 perimeter area/gate area)	Vertical	0.350	400	400	2200
.via2.1		Via2 (via2 area/gate area)	Horizontal		6	36	n/a
.met3.1		Met3 (met3 perimeter area/gate area)	Vertical	0.850	400	400	2200
.ar.1		Antenna rules not checked for features connected to a pAntennaShort					
Design limitations due to antenna rules (FET gate = 1um2).			w/o diode		with 1um2 diode		
Max length of Poly (approx, assumes min width)			135		n/a		
Max number of Licons			103		n/a		
Max length of LI (approx, assumes min width)			370		2620		
Max number of Mcon			103		726		
Max length of Met1 (approx, assumes min width)			570		4280		
Max number of Via			266		1866		
Max length of Met2 (approx, assumes min width)			570		4280		
Max number of Via2			76		535		
Max length of Met3 (approx, assumes min width)			230		1760		

Table 5.86: Table Ic. Antenna rules (S8TM-5R*/S8TMC-5R*/S8TMA-5R*)

Table Ic. Antenna rules (S8TM-5R*/S8TMC-5R*/S8TMA-5R*)						
	Antenna ratios	Area checked: H/V	FLT	MAX_EGA		
(ar_q.-.-)				Max EA/A w/o diode	K	Diode bonus
.poly.1	Poly (poly perimeter area/gate area)	Vertical	0.180	50	n/a	n/a
.licon.1	Licon (licon1 area/gate area)	Horizontal		3	n/a	n/a
.li.1	LI (LI perimeter area/gate area)	Vertical	0.100	75	450	n/a
.mcon.1	Mcon (mcon area/gate area)	Horizontal		3	18	n/a
.met1.1	Met1 (met1 perimeter area/gate area)	Vertical	0.350	400	400	2200
.via.1	Via (via area/gate area)	Horizontal		6	36	n/a
.met2.1	Met2 (met2 perimeter area/gate area)	Vertical	0.350	400	400	2200
.via2.1	Via2 (via2 area/gate area)	Horizontal		6	36	n/a
.met3.1	Met3 (met3 perimeter area/gate area)	Vertical	2.000	400	400	2200
.ar.1	Antenna rules not checked for features connected to a pAntennaShort					
Design limitations due to antenna rules (FET gate = 1um2).		w/o diode		with 1um2 diode		
Max length of Poly (approx, assumes min width)		135		n/a		
Max number of Licons		103		n/a		
Max length of LI (approx, assumes min width)		370		2620		
Max number of Mcon		103		726		
Max length of Met1 (approx, assumes min width)		570		4280		
Max number of Via		266		1866		
Max length of Met2 (approx, assumes min width)		570		4280		
Max number of Via2		9		65		
Max length of Met3 (approx, assumes min width)		95		740		

Table 5.87: Table Ie. Antenna rules (S8P-5R/SP8P-5R/S8P-

Table Ie. Antenna rules (S8P-5R/SP8P-5R/S8P-10R*)	
	Antenna ratios
(ar_q.-.-)	
.poly.1	Poly (poly perimeter area/gate area)
.licon.1	Licon (licon1 area/gate area)
.li.1	LI (LI perimeter area/gate area)
.mcon.1	Mcon (mcon area/gate area)
.met1.1	Met1 (met1 perimeter area/gate area)
.via.1	Via (via area/gate area)
.met2.1	Met2 (met2 perimeter area/gate area)
.via2.1	Via2 (via2 area/gate area)
.met3.1	Met3 (met3 perimeter area/gate area)
via3.1	Via3 (via3 area/gate area)
met4.1	Met4 (met4 perimeter area/gate area)
via4.1	Via3 (via3 area/gate area)
waffle_chip	Met4 (met4 perimeter area/gate area)
.ar.1	Antenna rules not checked for features connected to a pAntennaShort
Design limitations due to antenna rules (FET gate = 1um2).	
Max length of Poly (approx, assumes min width)	
Max number of Licons	
Max length of LI (approx, assumes min width)	
Max number of Mcon	
Max length of Met1 (approx, assumes min width)	
Max number of Via	
Max length of Met2 (approx, assumes min width)	
Max number of Via2	
Max length of Met3 (approx, assumes min width)	
Max number of Via3	
Max length of Met4 (approx, assumes min width)	
Max number of Via4	
Max length of Met5 (approx, assumes min width)	

Table 5.88: Table Ig. Antenna rules (S8P12-10R*/S8PIR-10R*)

Table Ig. Antenna rules (S8P12-10R*/S8PIR-10R/S8PF-10R*)	
	Antenna ratios
(ar_q.-.-)	
.poly.1	Poly (poly perimeter area/gate area)
.licon.1	Licon (licon1 area/gate area)
.li.1	LI (LI perimeter area/gate area)
.mcon.1	Mcon (mcon area/gate area)
.met1.1	Met1 (met1 perimeter area/gate area)
.via.1	Via (via area/gate area)
.met2.1	Met2 (met2 perimeter area/gate area)
.via2.1	Via2 (via2 area/gate area)
.met3.1	Met3 (met3 perimeter area/gate area)

Table lg. Antenna rules (S8P12-10R*/S8PIR-10R/S8PF-10R*)	
via3.1	Via3 (via3 area/gate area)
met4.1	Met4 (met4 perimeter area/gate area)
via4.1	Via3 (via3 area/gate area)
met5.1	Met4 (met4 perimeter area/gate area)
.ar.1	Antenna rules not checked for features connected to a pAntenn
Design limitations due to antenna rules (FET gate = 1um2).	
Max length of Poly (approx, assumes min width)	
Max number of Licons	
Max length of LI (approx, assumes min width)	
Max number of Mcon	
Max length of Met1 (approx, assumes min width)	
Max number of Via	
Max length of Met2 (approx, assumes min width)	
Max number of Via2	
Max length of Met3 (approx, assumes min width)	
Max number of Via3	
Max length of Met4 (approx, assumes min width)	
Max number of Via4	
Max length of Met5 (approx, assumes min width)	

5.12 Parasitic Layout Extraction

This table list layers and contacts included in SPICE models, and parasitic layers include in the AssuraLayout Extraction.

The modeled columns indicate sheets and contacts that are parasitic resistance/capacitance included in the model extraction measurements.

The CAD columns indicate sheets and contacts that are parasitics included in the schematic/layout RCX from Assura.

Table 5.89: Parasitic Extraction Table

Name	Description	Model Structure	Notes	Modeled RX Contacts	Sheets	Actual CAD RX Contacts	Sheets	RX Discrepancy	Modeled CX Sheet	Actual CX Sheet	CX Discrepancy
	All Periphery FETs	mXXXX d g s b w l m ad as pd ps nrd nrs		none	diff(min	li-con/mcc	diff(ext), m3	none	poly/lico	li/m1/m. m3	li-negligible
	20V NDE-FETs NON-ISO	xXXXX d g s b w l m ad as pd ps nrd nrs		none	diff(min	mcon/vi	diff(ext), m3	none	poly/lico	li/m1/m. m3	li-negligible
	20V NDE-FETs ISO	xXXXX d g s b w l m ad as pd ps nrd nrs		none	diff(min	mcon/vi	diff(ext), m3	none	poly/lico	li/m1/m. m3	li-negligible __model__parasitic
	20V PDE-FETs	xXXXX d g s b w l m ad as pd ps nrd nrs		none	diff(min	mcon/vi	diff(ext), m3	none	poly/lico	li/m1/m. m3/sky1	li-negligible _model__parasiti
	Cell FETs	NOT EXTRACT FROM LAYOUT		N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
	All Diodes	dXXXX n1 n2 area pj		licon	diff	li-con/mcc	poly/li/n m3	licon-negligib	Junction	li/m1/m. m3	none
	RF ESD Diodes	xesd_X n1 n2 area pj		li-con/mcc	li/m1/m.	via2	m3	none	li/m1/m.	m3	none
pnp_05	Parasitic PNP	qXXXX nc nb ne ns sky130_ m		li-con/mcc	diff/li	mcon/vi	li/m1/m. m3	li/mcon-neglible	na	li/m1/m. m3	none
	Parasitic PNP (5X)	qXXXX nc nb ne ns sky130_ m		li-con/mcc	diff/li	mcon/vi	li/m1/m. m3	li/mcon-neglible	na	li/m1/m. m3	none
npn_05	Parasitic	qXXXX nc nb		li-con/mcc	diff/li	mcon/vi	li/m1/m. m3	li/mcon-neglible	na	li/m1/m. m3	none

---

Note: The models includes M1/M2 capacitance. As a result of RCX extraction limitation M1/M2 routing over the varactor will have no capacitance extraction.

Routing and placement of devices over or under Precision resistors (xhrpoly_X_X) should be avoided.

The parasitic capacitance between 3-terminal MIMC and any routing/devices is not included in layout RCX, except M3 by 1 snap grid width.

No artificial fringing capacitance is extracted for MIMC M2/M3 due to CAD algorithm after CAPM sizing.

The parasitic capacitance between Precision resistors (xhrpoly_X_X) and any routing/devices is not included in layout RCX.

S8Q-5R is not supported for RF ESD diode RCX blocking.

The `areaid:substratecut` will be extracted as a 0.123 ohm two terms resistor.

5.12.1 Resistance Rules

Todo: This table should be rendered like the periphery rules.

Table 5.90: Table of resistance rules

	General (RES.-)	
.X	Parasitic resistance is not extrated under a sheet layer with it's corresponding res.id layer.	
	Sheet Resistance (SR.-)	
.X	Calibre now extracts deltaW by bucketing the sheet rho based on different widths.	The accuracy of each bucket must be within 2% of the Sheet Rho Calc using deltaW.
.met3	Parasitic resistance is calculated for all metal3 (if metal3 exists for the specific technology)	
.met2	Parasitic resistance is calculated for all metal2.	
.met1	Parasitic resistance is calculated for all metal1 with the exception of varactor which follow rule SR.xcnwvc.1	
.li1	Parasitic resistance is calculated for all li1.	
.poly	Parasitic resistance on gates is calculated to the center of the gate.	
.poly	Parasitic resistance for poly is not extracted beyond the device terminal. The device terminal for all devices but MOS is at the edge of the poly. Note: This means that parasitic resistance is not extracted for poly that is part of an LVS capacitor or LVS resistor. The LVS capacitors have poly in the model.	
.diff.1	Parasitic resistance is not extracted for any diffusion regions.	
.diff.2	Extract NRD/NRS for MOSFETs (except extendedDrain Fets) per the equations defined in USC-206. NRD/NRS for the n-type ESD devices must include the ntap enclosed in the source/drain ndiff hole NRD/NRS for the p-type ESD devices must include the ptap enclosed in the source/drain pdiff hole.	
.xnwvc.	Inside the Varactor device boundry (see rule PASSIVES.cnwvc.1) all layers listed in the model (m1 and below) will not have resistance extracted.	
	contact-to-gate space (CT.-)	
.via	All vias will have parasitic resistance extracted.	
.mcon	All mcons will have parasitic resistance extracted.	
.licon.1	All licons that are connected to Poly and not connected to the poly of the xhrpoly_X_X device should have resistance extracted.	
.licon.2	All licons that are connnected to non-precision resistors will have resistance extracted.	
.licon.3	All licons that are connected to FETs will be extracted by RCX.	
.licon.4	All licons on diff of PNP/NPN will be considered part of the device model.	
.licon.5	All licons on tap of PNP/NPN will be considered part of the device model.	
.licon.6	All licons on non-PNP tap regions will have parasitic resistance extracted.	
.hrpc	All licons and mcons that are part of the hrpoly resistor will not have parasitic resitance extracted, these contacts are in the models.	
.pwre	All licons and mcons that are part of the pwell resistor will not have parasitic resitance extracted, these contacts are in the models.	

5.12.2 Resistance Values

This section includes tables of basic resistance values for SKY130.

Further data can be found in the "SKY130 Stackup Capacitance Data" spreadsheet.

Table 5.91: Table - Resistances

Layer	Resistivity (mohms/sq)
Poly	48200
Local interconnect	12800
Metal1	125
Metal2	125
Metal3	47
Metal4	47
Metal5	29
Deep nwell	2200000
Pwell (in deep nwell)	3050000
Nwell	1700000
N-diffusion	120000
P-diffusion	197000
HV N-diffusion	114000
HV P-diffusion	191000
XHR poly resistor	319800
UHR poly resistor	2000000
LICON contact	15000
MCON contact	152000
VIA	4500
VIA2	3410
VIA3	3410
VIA4	380

5.12.3 Capacitance Rules

Todo: This table should be rendered like the periphery rules.

Table 5.92: Table of capacitance rules

General (CAP.-)		
.X.1	No capacitance is extracted due to contacts. (This is a generic layout extraction tool limitation.)	
MOS Devices (MOS.-)		
.mos.1	area between poly and diff should not have capacitance extracted.	
.mos.2	li within .055um will not have fringing capacitance (npcon.4 = 0.055 for S8)	
.mos.3	there will be no fringing caps between gates (as capacitance is shielded by the LICON and MCON).	
.mos.4	All 20V NMOS ISO DEFETs will have the parasitic diodes included in the models.	
.mos.5	All 20V NMOS ISO DEFETs will have the parasitic diode included in the models.	This model also includes the 5th terminal Drain-Psub diode (DeepNwell - Psub).
.mos.6	All 20V PMOS DEFETs will have the parasitic DeepNwell-Psub diode included in the CAD extraction.	
.mos.7	The only 20V DEFET instance parameter that the model uses from CAD extraction is m-factor.	The model will over-write all other instance parameters from CAD extraction.
Resistors (RES.-)		
.res.1	short devices must not have capacitance calculated across the device.	
.res.2	fuse devices must have capacitance extracted.	
.res.3	poly resistors that are not the precision poly resistors (xhrpoly_X_X) must have capacitance extracted.	
.res.4	metops that are merged must have capacitance extracted.	
.res.5	parasitic resistors for diff/nwell must have the junction diode extracted.	
.res.6	Poly precision resistors must not have the poly-psub parasitic capacitance extracted (RCX should also exclude head/tail poly-psub capacitance).	
.res.7	For Poly precision resistors xhrpoly_X_1, the device recognition layer is defined by growing the poly.rs AND rpm.dg layers 0.50 um(head/tail distance from ID layer) in all directions. Poly-Field/Diff/Well, and Poly-Poly, Poly-Li will not have capacitance extracted inside this device recognition layer.	
.res.8	For Poly precision resistors xhrpoly_X_2, the device recognition layer is defined by growing the poly.rs AND rpm.dg layers	

5.12.4 Capacitance Values

This section includes tables of basic capacitance values for SKY130.

Further data can be found in the "SKY130 Stackup Capacitance Data" spreadsheet.

Basic Capacitance - Fringe Downward

Fringe capacitances are a constant value per unit length and are approximations. Determined by creating a layout with a 5um x 10um rectangle of each layer over or under a much larger rectangle of the other layer. The fringe capacitance computed from the total given minus the parallel plate capacitance.

"downward direction" means that the larger plate is below the 5um x 10um plate.

The layer in the first column is always the layer with the 5um x 10um plate.

Table 5.93: Table - Capacitance - Fringe Downward

Interlayer fringe capacitance (downward direction) (aF/um)	Poly	Local inter-connect	Metal1	Metal2	Metal3	Metal4
Local interconnect	51.846					
Metal1	46.724	59.496				
Metal2	41.222	46.277	67.045			
Metal3	43.531	46.708	54.814	69.846		
Metal4	38.105	39.709	42.563	46.382	70.522	
Metal5	39.908	41.147	43.188	45.592	54.152	82.819

Basic Capacitance - Fringe Upward

Fringe capacitances are a constant value per unit length and are approximations. Determined by creating a layout with a 5um x 10um rectangle of each layer over or under a much larger rectangle of the other layer. The fringe capacitance computed from the total given minus the parallel plate capacitance.

"upward direction" means that the larger plate is above the 5um x 10um plate.

The layer in the first column is always the layer with the 5um x 10um plate.

Table 5.94: Table - Capacitance - Fringe Upward

Interlayer fringe capacitance (upward direction) (aF/um)	Local intercon-nect	Metal1	Metal2	Metal3	Metal4	Metal5
Poly	25.138	16.691	11.166	9.18	6.3505	6.4903
Local interconnect		34.7	21.739	15.078	10.141	7.6366
Metal1			48.193	26.676	16.421	12.017
Metal2				44.432	22.332	15.693
Metal3					42.643	27.836
Metal4						46.976

Basic Capacitance - Parallel

Table 5.95: Table - Capacitance - Parallel

Interlayer parallel plate capacitance (aF/um^2)	Local interconnect	Metal1	Metal2	Metal3	Metal4	Metal5
Poly	94.1644	44.8056	24.4968	16.0552	10.0131	7.2085
Local interconnect		114.1970	37.5647	20.7915	11.6705	8.0265
Metal1			133.8610	34.5350	15.0275	9.4789
Metal2				86.1861	20.3321	11.3410
Metal3					84.0346	19.6269
Metal4						68.3252

5.12.5 Discrepencies

Non-precision poly resistors

These resistors do not extract capacitance to substrate.

This needs to be accounted for manually by using ICPS_0150_0210 (cap per perimeter), and ICPS_2000_4000 (cap per area).

Un-shielded VPP's

Any routing above an un-shielded VPP will not be extracted.

The impact of this on total capacitance and parasitic capacitance is already comprehended in the model corners, however, cross-talk is not modeled. Also, parasitic cap is routed to ground and this may not be ideal for the scenario. The parasitic cap can be estimated using RescapWeb.

5.13 Device Details

5.13.1 1.8V NMOS FET

Spice Model Information

- Cell Name: sky130_fd_pr__nfet_01v8

- Model Name: sky130_fd_pr__nfet_01v8

Operating Voltages where SPICE models are valid

- V_{DS} = 0 to 1.95V

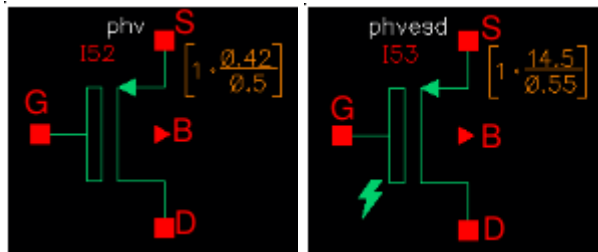- V_{GS} = 0 to 1.95V

- V_{BS} = +0.3 to -1.95V

Details

Major model output parameters are shown below and compared against the EDR (e-test) specs.

Parameter	W/L	Units	MODEL TT	FF	SS	FS	SF	EDR NOM	MIN	MAX
VTXNL	7/8	V	0.538	0.520	0.557	0.513	0.564	0.541	0.515	0.567
VTXNN42	0.42/1	V	0.550	0.522	0.578	0.510	0.590	0.550	0.510	0.590
VTXNS15	7/0.15	V	0.645	0.615	0.677	0.603	0.689	0.700	0.661	0.739
VT-SNSN15	0.42/0.15	V	0.738	0.659	0.818	0.625	0.852	0.738	0.625	0.852
IDSNS15	7/0.15	mA	3.512	3.945	3.078	3.041	3.983	3.510	3.039	3.981
ILKN15	7/0.15	LOG A	Max = -10.25	-11.31	-18	-10.69				

The symbol of the sky130_fd_pr__nfet_01v8 (1.8V NMOS FET) is shown below:
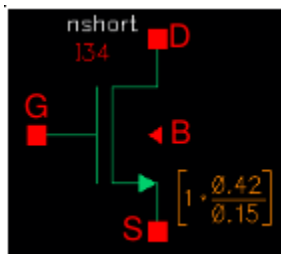
The cross-section of the NMOS FET is shown below:
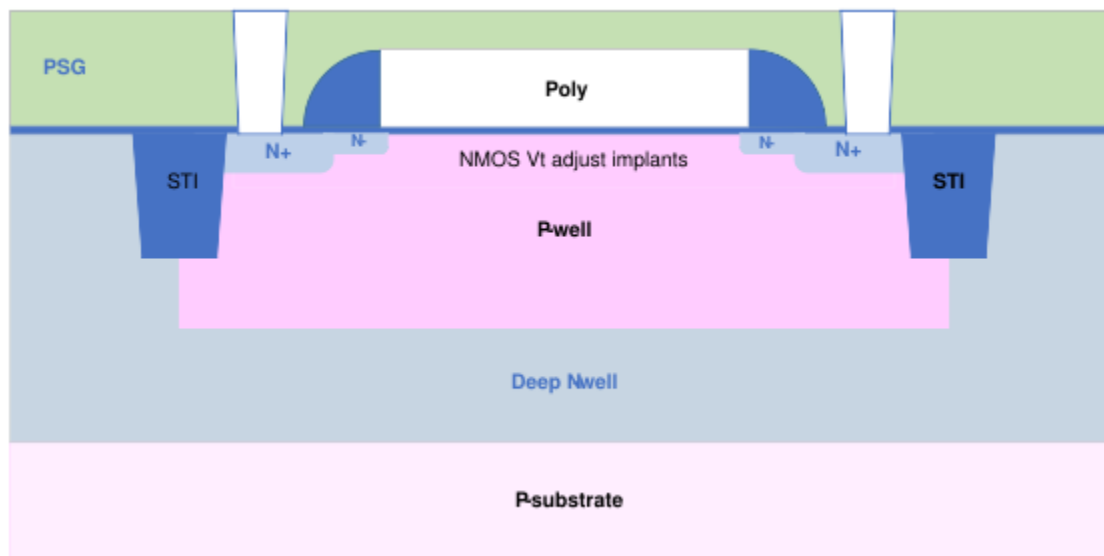
The device shows the p-well inside of a deep n-well, but it can be made either with or without the DNW under the p-well

5.13.2 1.8V low-VT NMOS FET

Spice Model Information

- Cell Name: sky130_fd_pr__nfet_01v8
- Model Name: sky130_fd_pr__nfet_01v8_lvt

Operating Voltages where SPICE models are valid

- $V_{DS} = 0$ to 1.95V
- $V_{GS} = 0$ to 1.95V
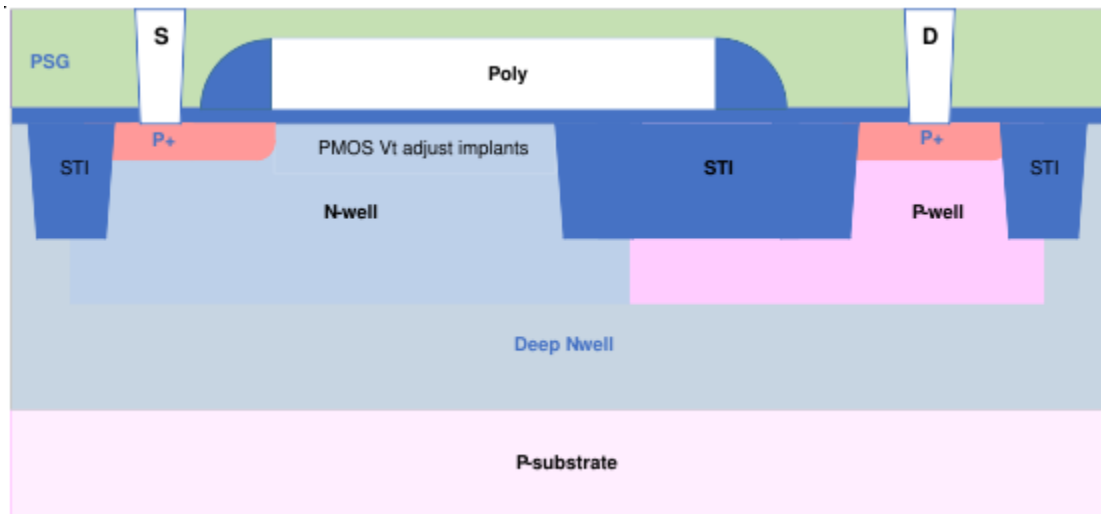- $V_{BS} = +0.3$ to -1.95V

Details

Major model output parameters are shown below and compared against the EDR (e-test) specs.

Parameter	W/L	Units	MODEL TT	FF	SS	FS	SF	EDR NOM	MIN	MAX
VTXNLL	7/8	V	0.434	0.417	0.452	0.459	0.410	0.440	0.415	0.465
VTXNN42L	0.42/1	V	0.485	0.453	0.516	0.530	0.440	0.485	0.440	0.530
VTXNS15L	7/0.15	V	0.611	0.573	0.65	0.666	0.556	0.611	0.556	0.666
VTXNSN15L	0.42/0.15	V	0.640	0.562	0.717	0.750	0.529	0.640	0.529	0.750
IDSNS15L	7/0.15	mA	4.010	4.453	3.567	3.529	4.491	4.008	3.527	4.489
ILKN15L	7/0.15	LOG A	Max = -9.53	-10.73	-18	-9.54				

Inverter Gate Delays using sky130_fd_pr__nfet_01v8_lvt/sky130_fd_pr__pfet_01v8 device combinations:

Parameter	Stages	Units	MODEL TT	FF	SS	EDR NOM	MIN	MAX
FO = 1	143	ps				28.61	21.96	39.15

The symbol of the sky130_fd_pr__nfet_01v8_lvt (1.8V low-VT NMOS FET) is shown below:
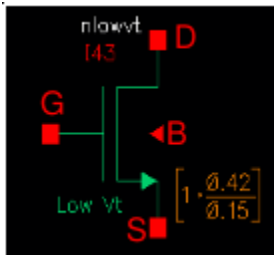
The cross-section of the low-VT NMOS FET is shown below. The cross-section is identical to the std NMOS FET except for the V_T adjust implants (to achieve the lower V_T)
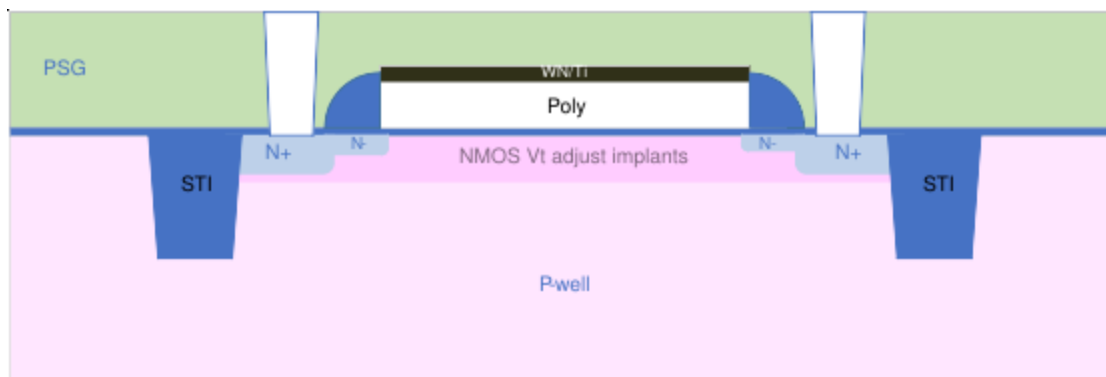
5.13.3 1.8V PMOS FET

Spice Model Information

- Cell Name: sky130_fd_pr__pfet_01v8
- Model Name: sky130_fd_pr__pfet_01v8

Operating Voltages where SPICE models are valid

- $V_{DS} = 0$ to -1.95V
- $V_{GS} = 0$ to -1.95V
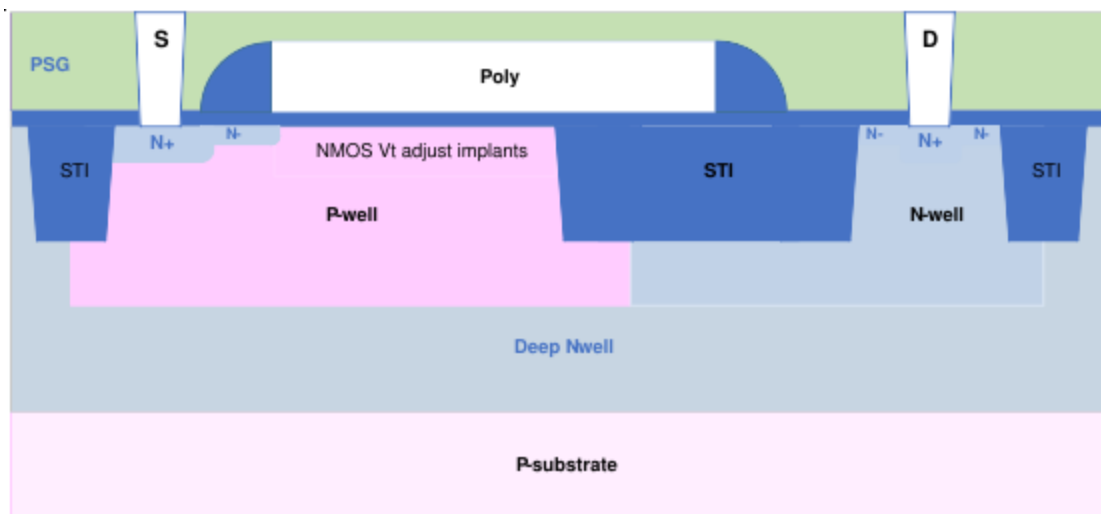- $V_{BS} = -0.1$ to +1.95V

Details

Major model output parameters are shown below and compared against the EDR (e-test) specs.

Parameter	W/L	Units	MODEL TT	FF	SS	FS	SF	EDR NOM	MIN	MAX
VTXPLS	7/8	V	-1.050	-1.025	-1.075	-1.014	-1.086	-1.050	-1.086	-1.014
VTXPN42S	0.42/8	V	-0.941	-0.910	-0.960	-0.895	-0.983	-0.941	-0.985	-0.895
VTXPS15S	7/0.15	V	-0.781	-0.728	-0.835	-0.705	-0.858	-0.781	-0.858	-0.705
VTX-PSN15S	0.42/0.15	V	-0.705	-0.599	-0.811	-0.554	-0.856	-0.705	-0.856	-0.554
IDSPS15S	7/0.15	mA	1.347	1.742	0.952	0.917	1.777	1.347	0.917	1.777
ILKP15S	7/0.15	LOG A	Max -7.58	= -10.09	-18	-7.58				

Inverter Gate Delays using sky130_fd_pr__nfet_01v8/sky130_fd_pr__pfet_01v8 device combinations:

Parameter	Stages	Units	MODEL TT	FF	SS	EDR NOM	MIN	MAX
FO = 1	143	ps				31.8	24.7	44.1

The symbol of the sky130_fd_pr__pfet_01v8 (1.8V PMOS FET) is shown below:

.
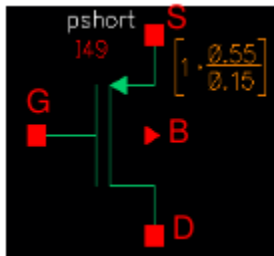
The cross-section of the PMOS FET is shown below:

.
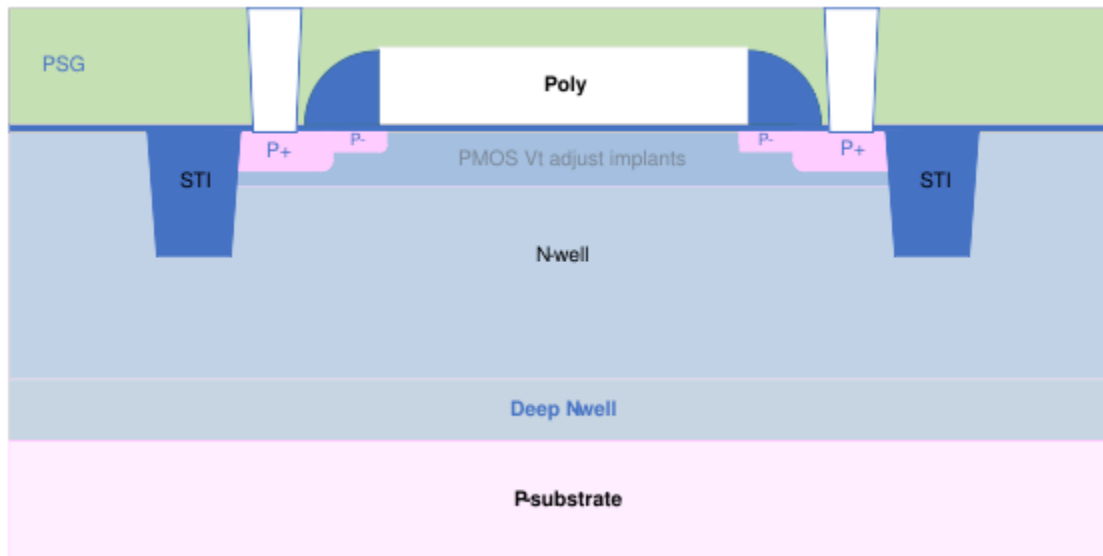
5.13.4 1.8V low-VT PMOS FET

Spice Model Information

- Cell Name: sky130_fd_pr__pfet_01v8
- Model Name: sky130_fd_pr__pfet_01v8_lvt

Operating Voltages where SPICE models are valid

- $V_{DS} = 0$ to -1.95V
- $V_{GS} = 0$ to -1.95V
- $V_{BS} = -0.1$ to +1.95V

Details

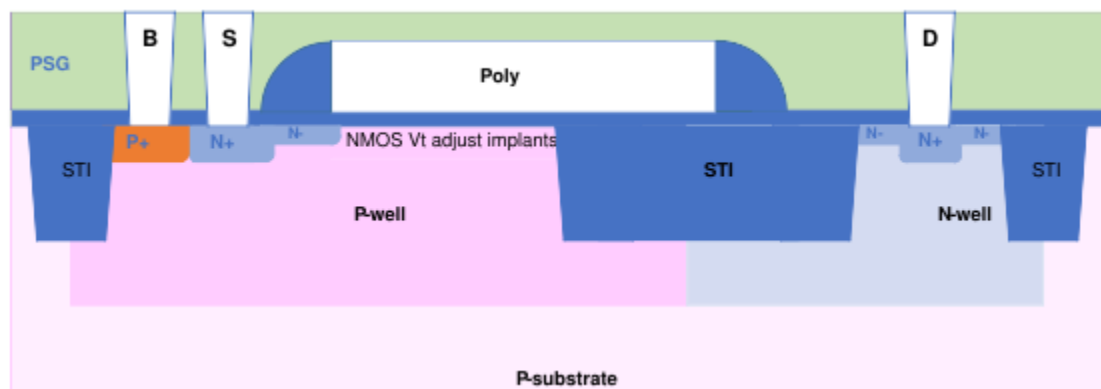Major model output parameters are shown below and compared against the EDR (e-test) specs

Parameter	W/L	Units	MODEL TT	FF	SS	FS	SF	EDR NOM	MIN	MAX
VTCPLL	7/8	V	-0.651	-0.558	-0.744	-0.518	-0.784	-0.651	-0.785	-0.518
VTCPN42L	0.42/8	V	-0.630	-0.527	-0.733	-0.483	-0.777	-0.630	-1.042	-0.845
VTCPS35L	7/0.35	V	-0.533	-0.428	-0.638	-0.384	-0.683	-0.533	-0.683	-0.384
VTCPSN35L	0.42/0.35	V	-0.504	-0.373	-0.636	-0.316	-0.693	-8.505	-0.693	-0.316
IDSPS35L	7/0.35	mA	1.22	1.42	1.02	1.44	1.00	1.22	1.00	1.44
ILKP35L	7/0.35	LOG A	Max -5.14	= -6.671	-18	-5.144				

Inverter Gate Delays using sky130_fd_pr__nfet_01v8_lvt/sky130_fd_pr__pfet_01v8_lvt device combinations:

Parameter	Stages	Units	MODEL TT	FF	SS	EDR NOM	MIN	MAX
FO = 1	99	ps				43.4	35.9	54.8

The symbol of the sky130_fd_pr__pfet_01v8_lvt (1.8V low-VT PMOS FET) is shown below:
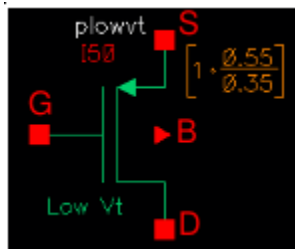
The cross-section of the low-VT PMOS FET is shown below. The cross-section is identical to the std PMOS FET except for the V_T adjust implants (to achieve the lower V_T)
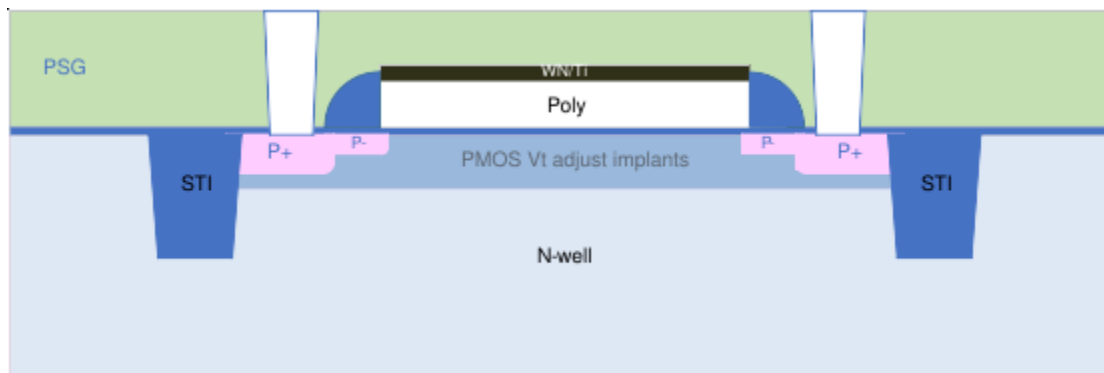
5.13.5 1.8V high-VT PMOS FET

Spice Model Information

- Cell Name: sky130_fd_pr__pfet_01v8
- Model Name: sky130_fd_pr__pfet_01v8_hvt

Operating Voltages where SPICE models are valid

- $V_{DS} = 0$ to -1.95V
- $V_{GS} = 0$ to -1.95V
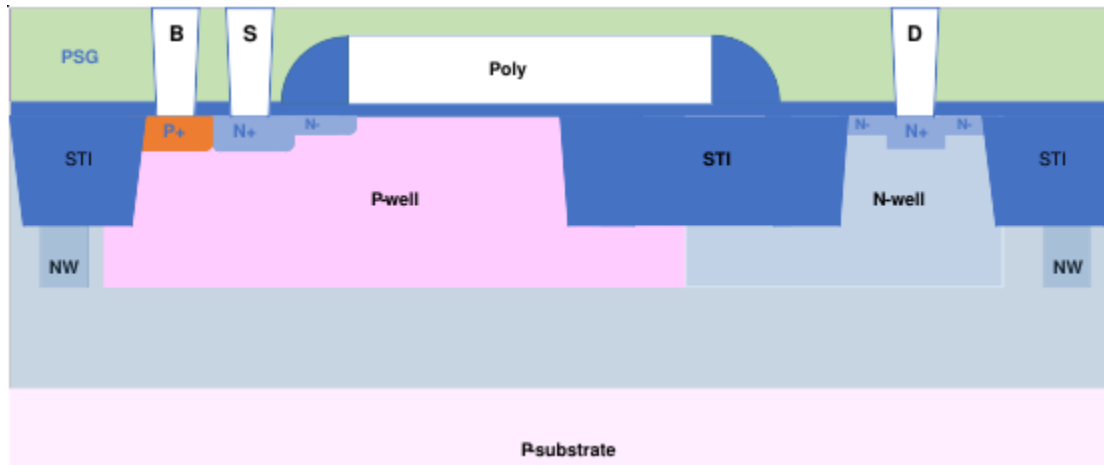- $V_{BS} = -0.1$ to +1.95V

Details

Major model output parameters are shown below and compared against the EDR (e-test) specs

Parameter	W/L	Units	MODEL TT	FF	SS	FS	SF	EDR NOM	MIN	MAX
VTXPL	7/8	V	-1.107	- 1.079	- 1.124	-1.067	- 1.141	- 1.107	- 1.141	- 1.067
VTXPN42	0.42/8	V	-1.013	- 0.974	- 1.049	-0.959	- 1.056	- 1.023	- 1.056	- 0.959
VTXPS15	7/0.15	V	-0.888	- 0.836	- 0.940	-0.814	- 0.962	- 0.888	- 0.963	- 0.814
VTX-PSN15	0.42/0.15	V	-0.819	- 0.720	- 0.918	-0.678	- 0.951	- 0.819	- 0.951	- 0.678
IDSPS15	7/0.15	mA	1.003	1.285	0.721	1.309	0.697	1.003	0.697	1.309
ILKP15	7/0.15	LOG A	Max -10.7	= -12	-18	- 10.787				

Inverter Gate Delays using sky130_fd_pr__nfet_01v8/sky130_fd_pr__pfet_01v8_hvt device combinations:

Parameter	Stages	Units	MODEL TT	FF	SS	EDR NOM	MIN	MAX
FO = 1	143	ps				38	29.3	52.1

The symbol of the sky130_fd_pr__pfet_01v8_hvt (1.8V high-VT PMOS FET) is shown below:
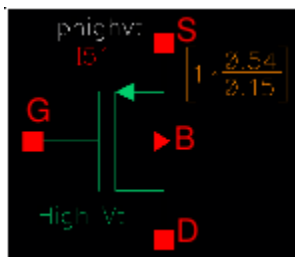
The cross-section of the high-VT PMOS FET is shown below. The cross-section is identical to the std PMOS FET except for the V_T adjust implants (to achieve the higher V_T)
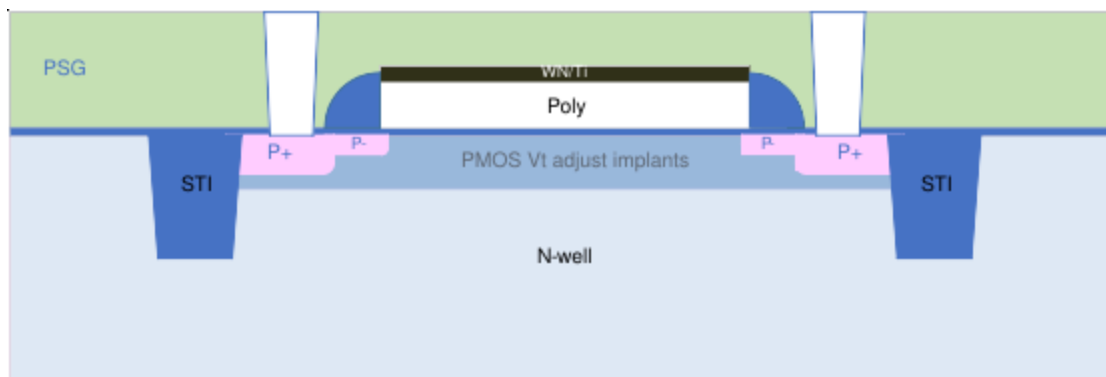
5.13.6 1.8V accumulation-mode MOS varactors

Spice Model Information

- Cell Name: **:cell:`capbn_b`**
- Model Name: sky130_fd_pr__cap_var_lvt, sky130_fd_pr__cap_var_hvt
- Model Type: subcircuit

Operating Voltages where SPICE models are valid

- $|V_0 \check{} V_1| = 0$ to 2.0V

Details

The following devices are available; they are subcircuits with the N-well to P-substrate diodes built into the model:

- sky130_fd_pr__cap_var_lvt - low VT PMOS device option
- sky130_fd_pr__cap_var_hvt - high VT PMOS device option

The varactors are used as tunable capacitors, major e-test parameters are listed below. Further details on the device models and their usage are in the SKY130 process Family Spice Models (002-21997), which can be obtained from SkyWater upon request.

Parameter	NOM	LSL	USL	Units	Description
VC_CMAX_5_5	20.26	18.91	21.52	pF	PLOWVT based varactor 5/5 in accumulation
VC_CMAX_5_P5	10.17	9.21	11.12	pF	PLOWVT based varactor 5/5 in inversion
VC_CMIN_5_5	2.058	1.863	2.262	pF	PLOWVT based varactor 5/0.5 in accumulation
VC_CMIN_5_P5	1.9	1.725	2.087	pF	PLOWVT based varactor 5/0.5 in inversion
VC2_CMAX_5_5	20.37	19.02	21.68	pF	PHIGHVT based varactor 5/5 in accumulation
VC2_CMAX_5_P5	10.2	9.24	11.18	pF	PHIGHVT based varactor 5/5 in inversion
VC2_CMIN_5_5	4.197	3.95	4.453	pF	PHIGHVT based varactor 5/0.5 in accumulation
VC2_CMIN_5_P5	2.762	2.537	2.999	pF	PHIGHVT based varactor 5/0.5 in inversion

There is no equivalent varactor for 5V operation. The NHV or PHV devices should be connected as capacitors for use at 5V.

The symbols for the varactors are shown below:
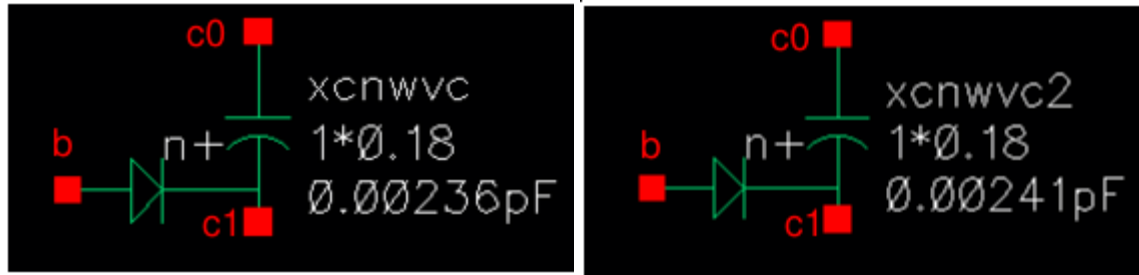
The cross-section of the varactor is shown below:
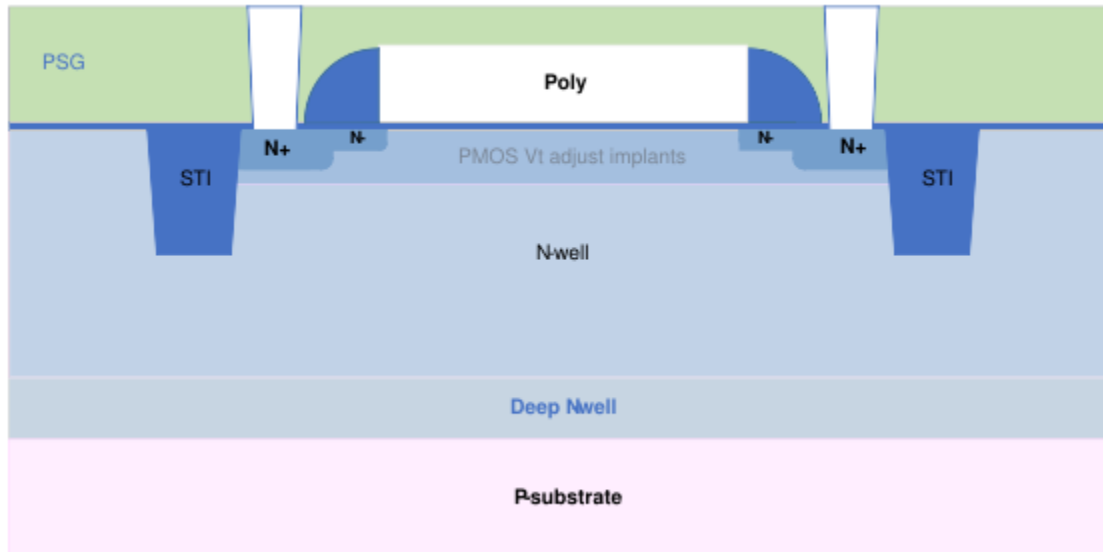
5.13.7 3.0V native NMOS FET

Spice Model Information

- Cell Name: sky130_fd_pr__nfet_01v8
- Model Name: sky130_fd_pr__nfet_03v3_nvt

Operating Voltages where SPICE models are valid for sky130_fd_pr__nfet_03v3_nvt

- $V_{DS} = 0$ to 3.3V
- $V_{GS} = 0$ to 3.3V
- $V_{BS} = 0$ to -3.3V

Details

The native device is constructed by blocking out all VT implants.

The model and EDR (e-test) parameters are compared below. Note that the minimum gate length for 3V operation is 0.5 μm.

Param	W/L	Units	MODEL TT	FF	SS	FS	SF	EDR NOM	MIN	MAX
VTXNLNVH	10/4.0	V	0.121	0.091	0.151	0.164	0.079	0.121	0.079	0.164
VTXNS90NVH	10/0.9	V	5.855	6.098	5.605	6.107	5.592	0.097	0.044	0.150
VTXNSN90NVH	0.42/0.9	V	0.075	0.017	0.129	0.152	-0.014	0.075	-0.002	0.152
IDSNS90NTH	10/0.9	mA	0.097	0.06	0.134	0.15	0.044	5.819	5.558	6.069
ILKN90NVH	10/0.9	LOG A	Max = -5.6	-6.5	-18	-5.6				
VTXNS50NTH	10/0.5	V	-0.029	0.029	0.013	0.031	0.011	-0.029	-0.089	0.031
VTXNSN50NTH	0.42/0.5	V	-0.033	0.013	0.02	0.043	-0.009	-0.046	-0.142	0.050
IDSNS50NTH	10/0.5	mA	4.858	5.294	4.423	5.331	4.386	4.823	4.357	5.291
ILKN50NVH	10/0.5	LOG A	Max = -3.6	-4.03	-18	-3.67				

The symbols for the sky130_fd_pr__nfet_03v3_nvt devices are shown below.
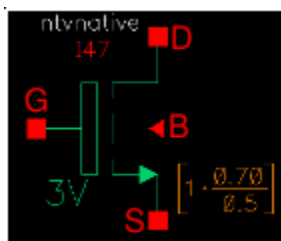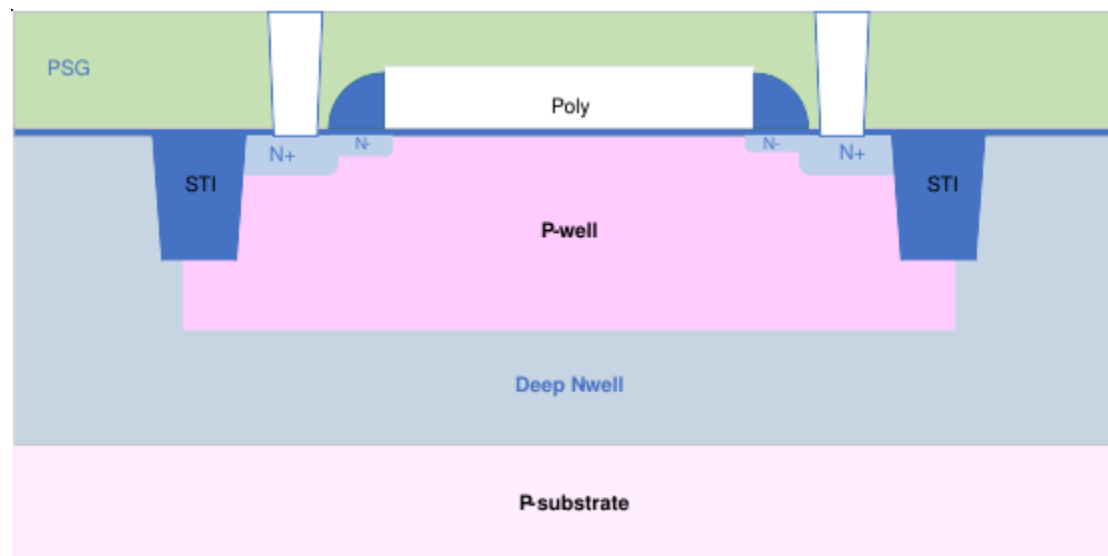
The cross-section of the native devices is shown below.

Note: The only differences between the sky130_fd_pr__nfet_03v3_nvt and sky130_fd_pr__nfet_05v0_nvt devices are the minimum gate length and the VDS requirements.

5.13.8 5.0V native NMOS FET

Spice Model Information

- Cell Name: sky130_fd_pr__nfet_05v0_nvt
- Model Name: sky130_fd_pr__nfet_05v0_nvt

Operating Voltages where SPICE models are valid for sky130_fd_pr__nfet_05v0_nvt

- $V_{DS} = 0$ to 5.5V
- $V_{GS} = 0$ to 5.5V
- $V_{BS} = +0.3$ to -5.5V

Details

The native device is constructed by blocking out all VT implants.

The model and EDR (e-test) parameters are compared below.

The 5V device has minimum gate length of 0.9 μm.

Param	W/L	Units	MODEL TT	FF	SS	FS	SF	EDR NOM	MIN	MAX
VTXNLNVH	10/4.0	V	0.121	0.091	0.151	0.164	0.079	0.121	0.079	0.164
VTXNS90NVH	10/0.9	V	5.855	6.098	5.605	6.107	5.592	0.097	0.044	0.150
VTXNSN90NVH	0.42/0.9	V	0.075	0.017	0.129	0.152	-0.014	0.075	-0.002	0.152
IDSNS90NTH	10/0.9	mA	0.097	0.06	0.134	0.15	0.044	5.819	5.558	6.069
ILKN90NVH	10/0.9	LOG A	Max = -5.6	-6.5	-18	-5.6				
VTXNS50NTH	10/0.5	V	-0.029	0.029	0.013	0.031	0.011	-0.029	-0.089	0.031
VTXNSN50NTH	0.42/0.5	V	-0.033	0.013	0.02	0.043	-0.009	-0.046	-0.142	0.050
IDSNS50NTH	10/0.5	mA	4.858	5.294	4.423	5.331	4.386	4.823	4.357	5.291
ILKN50NVH	10/0.5	LOG A	Max = -3.6	-4.03	-18	-3.67				

The symbols for the sky130_fd_pr__nfet_05v0_nvt devices are shown below.

The cross-section of the native devices is shown below.

Note: The only differences between the sky130_fd_pr__nfet_03v3_nvt and sky130_fd_pr__nfet_05v0_nvt devices are the minimum gate length and the VDS requirements.

5.13.9 5.0V/10.5V NMOS FET

Spice Model Information

- Cell Name: sky130_fd_pr__nfet_01v8
- Model Name: sky130_fd_pr__nfet_g5v0d10v5

Operating Voltages where SPICE models are valid

- $V_{DS} = 0$ to 11.0V
- $V_{GS} = 0$ to 5.5V
- $V_{BS} = 0$ to -5.5V

Details

Major model output parameters are shown below and compared against the EDR (e-test) specs

Param	W/L	Units	MODEL TT	FF	SS	FS	SF	EDR NOM	MIN	MAX
VTXNLH	7/8	V	0.811	0.780	0.843	0.856	0.767	0.811	0.767	0.856
VTXNN42H	0.42/20	V	0.813	0.764	0.862	0.883	0.743	0.813	0.743	0.883
VTXNS50H	7/0.50	V	0.822	0.744	0.899	0.933	0.711	0.822	0.711	0.933
VTXNSN50H	0.42/0.50	V	0.781	0.672	0.891	0.937	0.625	0.781	0.625	0.937
IDSNS50H	7/0.50	mA	12.1	13.0	11.2	11.1	13.1	12.1	11.1	13.1
ILKN50H	7/0.50	LOG A	Max = -10.6	-12.3	-18	-10.9				

The symbols of the sky130_fd_pr__nfet_g5v0d10v5 (5.0/10.5 V NMOS FET) is shown below:
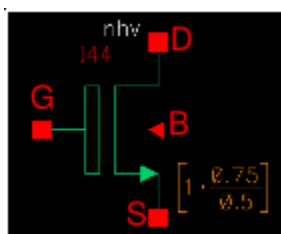
The cross-section of the 5.0/10.5 V NMOS FET is shown below.
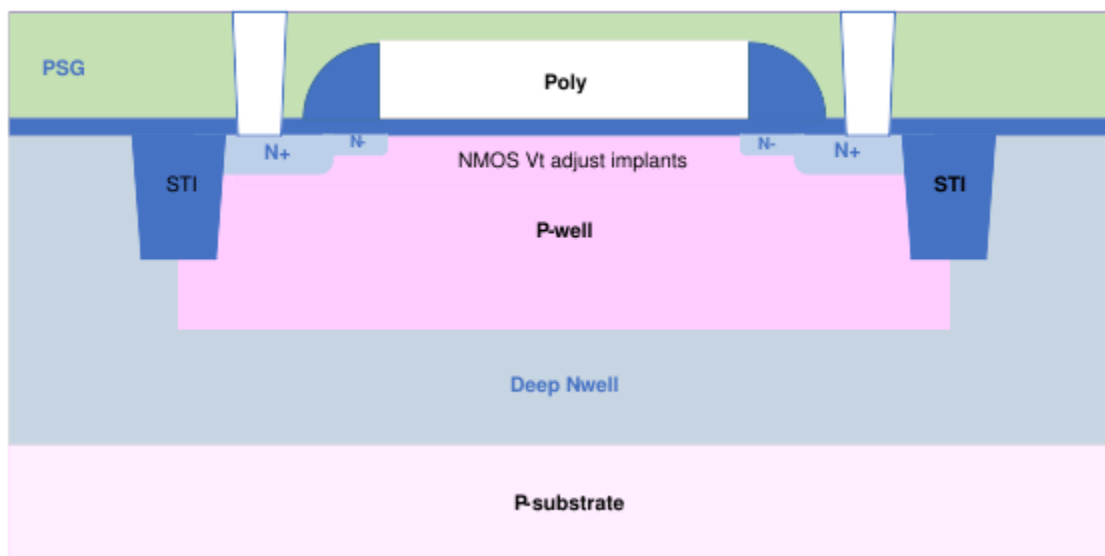
5.13.10 5.0V/10.5V PMOS FET

Spice Model Information

- Cell Name: sky130_fd_pr__pfet_01v8
- Model Name: sky130_fd_pr__pfet_g5v0d10v5, sky130_fd_pr__esd_pfet_g5v0d10v5

Operating Voltages where SPICE models are valid

- $V_{DS} = 0$ to -11.0V
- $V_{GS} = 0$ to -5.5V
- $V_{BS} = 0$ to +5.5V

Details

Major model output parameters are shown below and compared against the EDR (e-test) specs

Param	W/L	Units	MODEL TT	FF	SS	FS	SF	EDR NOM	MIN	MAX
VTXPLH	7/8	V	-1.027	-0.971	-1.083	-0.947	-1.107	-1.027	-1.107	-0.947
VTXPN42H	0.42/20	V	-0.933	-0.886	-0.979	-0.867	-0.998	-0.93	-1.00	-0.87
VTXPS50H	7/0.50	V	-0.956	-0.889	-1.022	-0.861	-1.05	-0.954	-1.049	-0.859
VTX-PSN50H	0.42/0.50	V	-0.832	-0.737	-0.927	-0.697	-0.968	-0.831	-0.967	-0.695
IDSPS50H	7/0.50	mA	7.02	7.75	6.30	6.24	7.809	6.83	6.07	7.59
ILKPS50H	7/0.50	LOG A	Max -10.0	= -10.6	-18	-10				

Inverter gate delays are shown below:

Parameter	Stages	Units	MODEL TT	FF	SS	EDR NOM	MIN	MAX
FO = 1	79	ps				53.87	46.68	62.83

The symbols of the sky130_fd_pr__pfet_g5v0d10v5 and sky130_fd_pr__esd_pfet_g5v0d10v5 (5.0V/10.5V PMOS FET) are shown below:

The cross-section of the 5.0V PMOS FET is shown below.
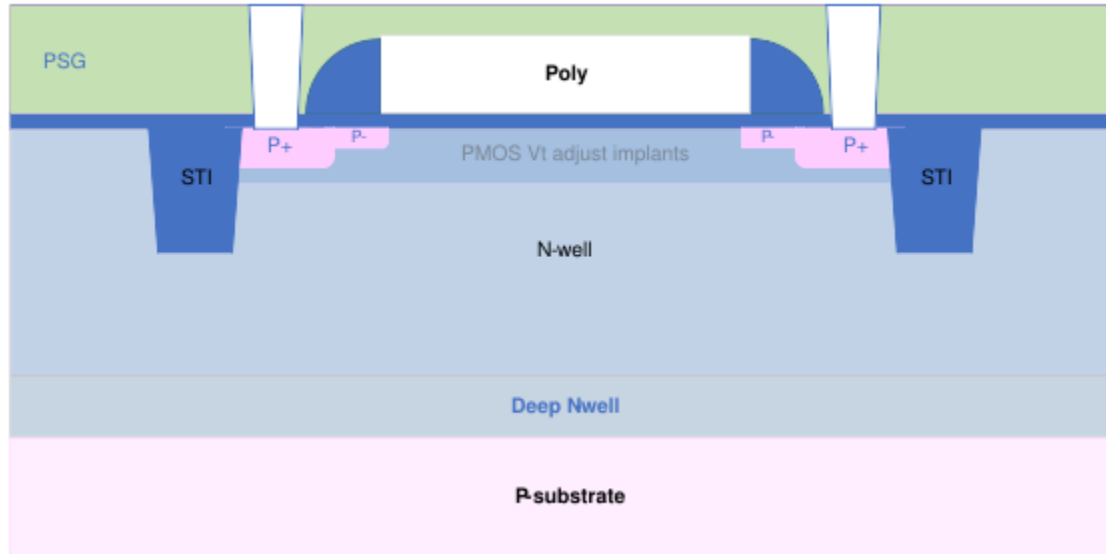
5.13.11 10V/16V PMOS FET

Spice Model Information

- Cell Name: sky130_fd_pr__pfet_extenddrain
- Model Name: sky130_fd_pr__pfet_g5v0d16v0

Operating Voltages where SPICE models are valid, subject to SOA limitations:

- $V_{DS} = 0$ to -16V ($V_{GS} = 0$)
- $V_{DS} = 0$ to -10V ($V_{GS} < 0$)
- $V_{GS} = 0$ to -5.5V
- $V_{BS} = 0$ to +2.0V

Details

Major model output parameters are shown below and compared against the EDR (e-test) specs

Param	W/L	Units	MODEL TT	FF	SS	FS	SF	EDR NOM	MIN	MAX
VTX-PVHV20P00P66	20/0.66	V	-1.105	-1.015	-1.196	-0.975	-1.235	-1.10	-1.24	-0.98
VTX-PVHV20P02P20	20/2.2	V	-1.098	-1.006	-1.189	-0.967	-1.229	-1.10	-1.23	-0.97
ID-SPVHV20P00P66	20/0.66	mA	4.912	6.258	3.593	6.393	3.505	4.911	3.505	6.393
ID-SPVHV20P02P20	20/2.2	mA	1.902	2.403	1.392	2.448	1.343	1.902	1.343	2.448
RD-SPVHV20P00P66	20/0.66	Ω	754.8	483.1	1269.0	1274.7	481.6	757.1	482.9	1279
RD-SPVHV20P02P20	20/2.2	Ω	1407	1021	2128	2163	1015	1409	1016	2167
ILKPVHV20P00P66	20/0.66	LOG A	Max -9.66	=	-13.20	-14.55	-9.77			
ILKPVHV20P02P20	20/2.2	LOG A	Max -10.07	=	-13.20	-14.41	-10.42			

The symbol of the sky130_fd_pr__pfet_g5v0d16v0 (10V/16V PMOS FET) is shown below:
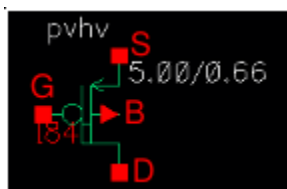
The cross-section of the 10V/16V PMOS FET is shown below.

5.13.12 11V/16V NMOS FET

Spice Model Information

- Cell Name: sky130_fd_pr__nfet_extenddrain
- Model Name: sky130_fd_pr__nfet_g5v0d16v0

Operating Voltages where SPICE models are valid, subject to SOA limitations:

- $V_{DS} = 0$ to +16V ($V_{GS} = 0$)
- $V_{DS} = 0$ to +11V ($V_{GS} > 0$)
- $V_{GS} = 0$ to 5.5V
- $V_{BS} = 0$ to -2.0V

Details

Major model output parameters are shown below and compared against the EDR (e-test) specs

Parameter	W/L	Units	MODEL TT	FF	SS	FS	SF	EDR NOM	MIN	MAX
VTXN-VHV20P00P7D	20/0.7	V	0.743	0.616	0.87	0.924	0.562	0.7423	0.5612	0.9234
VTXN-VHV20P02P2D	20/2.2	V	0.767	0.661	0.874	0.919	0.615	0.7668	0.6150	0.9191
ID-SNVHV20P00P7D	20/0.7	mA	9.012	11.337	6.68	11.542	6.477	8.969	6.430	11.51
ID-SNVHV20P02P2D	20/2.2	mA	4.444	5.56	3.329	5.657	3.232	4.440	3.232	5.656
RD-SNVHV20P00P7D	20/0.7	Ω	457.3	266.1	819.4	826.4	269.6	458.5	270.3	828.2
RD-SNVHV20P02P2D	20/2.2	Ω	702.8	499.7	1087.8	1097.7	498.7	703.8	499.3	1099.0
ILKN-VHV20P00P7D	20/0.7	LOG A	Max = - 9.01	- 11.35	-18	-9.05				
ILKN-VHV20P00P7D	20/2.2	LOG A	Max = - 9.44	- 11.50	-18	-9.50				

The symbol of the sky130_fd_pr__nfet_g5v0d16v0 (11V/16V NMOS FET) is shown below:
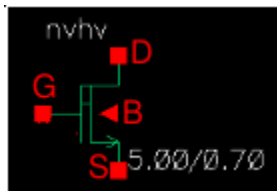
The cross-section of the 11V/16VV NMOS FET is shown below.

5.13.13 20V NMOS FET

Spice Model Information

- Cell Name: sky130_fd_pr__nfet_extenddrain
- Model Name: sky130_fd_pr__nfet_20v0

Operating Voltages where SPICE models are valid, subject to SOA limitations:

- $V_{DS} = 0$ to +22V
- $V_{GS} = 0$ to 5.5V
- $V_{BS} = 0$ to -2.0V

Details

The 20V NMOS FET has similar construction to the 11V/16V NMOS FET, with several differences:

- Longer drift region
- Longer poly gate
- Larger W/L
- Devices placed in pairs (drain in center, sources on outside)

Major model output parameters are shown below and compared against the EDR (e-test) specs

Param	W/L	Units	MODEL TT	FF	SS	FS	SF	EDR NOM	MIN	MAX
VTXN20VHV1	2* 30/1.0	V	0.823	0.643	1.004	1.004	0.643	0.8231	0.6432	1.004
VTBN20VHV1	2* 30/1.0	V	1.823	1.573	2.075	2.075	1.573	1.823	1.573	2.075
BVN20VHV1	2* 30/1.0	V						65.96	40	80
IBB20N20VHV1	2* 30/1.0	µA/µm						0.1623	0	0.6
ID5N20VHV1	2* 30/1.0	mA	1.537	2.579	0.892	0.892	2.579	1.528	0.8892	2.556
IDLN20VHV1	2* 30/1.0	mA	0.335	0.577	0.191	0.191	0.577	0.3326	0.1903	0.5709
IDSN20VHV1	2* 30/1.0	mA	13.35	17.34	9.34	9.34	17.34	13.34	9.335	17.34
RDSN20VHV1	2* 30/1.0	Ω	327.2	195.6	562.3	562.3	195.6	327.2	195.6	562.3
RSPON20VHV1	2* 30/1.0	mΩ-mm2	98.6	58.9	169.4	169.4	58.9	98.49	59.1	137.9
ILKN20VHV1	2* 30/1.0	LOG A	Max = -8.6	-11.63	-18	-8.162				

The symbol of the sky130_fd_pr__nfet_20v0 (20V NMOS FET) is shown below.
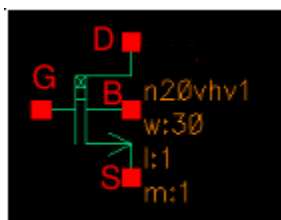
The cross-section of the 20V NMOS FET is shown below.

5.13.14 20V native NMOS FET

Spice Model Information

- Cell Name: sky130_fd_pr__nfet_extenddrain
- Model Name: sky130_fd_pr__nfet_20v0_nvt

Operating Voltages where SPICE models are valid, subject to SOA limitations:

- $V_{DS} = 0$ to +22V
- $V_{GS} = 0$ to 5.5V
- $V_{BS} = 0$ to -2.0V

Details

The 20V native NMOS FET is similar to the 20V isolated NMOS FET, but has all Vt implants blocked to achieve a very low VT.

Major model output parameters are shown below and compared against the EDR (e-test) specs

Param	W/L	Units	MODEL TT	FF	SS	FS	SF	EDR NOM	MIN	MAX
VTXN20VHV1L	2* 30/1.0	V	0.246	0.068	0.428	0.428	0.068	0.246	0.0676	0.4276
VTBN20VHV1L	2* 30/1.0	V	0.722	0.529	0.962	0.962	0.529	0.6321	0.436	0.8534
BVN20VHV1L	2* 30/1.0	V						58.19	40	80
IBB20N20VHV1L	2* 30/1.0	µA/µm						0.3764	0	0.6
ID5N20VHV1L	2* 30/1.0	mA	1.621	2.197	1.086	1.086	2.197	1.612	1.082	2.18
IDLN20VHV1L	2* 30/1.0	mA	0.366	0.492	0.247	0.247	0.492	0.3638	0.246	0.4872
IDSN20VHV1L	2* 30/1.0	mA	14.44	18.8	10.1	10.1	18.8	14.44	10.1	18.8
RDSP20VHV1L	2* 30/1.0	Ω	310.2	229.3	462.0	462.0	229.3	310.2	229.4	462
RSPOP20VHV1L	2* 30/1.0	mΩ-mm^2	93.4	69.1	139.1	139.1	69.1	89.63	69.01	128.2
ILKN20VHV1L	2* 30/1.0	LOG A	Max = -5.6	- -7.463	- 9.403	- 5.607				

The symbol of the sky130_fd_pr__nfet_20v0_nvt (20V native NMOS FET) shown below.

The cross-section of the 20V native NMOS FET is shown below.

5.13.15 20V zero-VT NMOS FET

Spice Model Information

- Cell Name: sky130_fd_pr__nfet_extenddrain
- Model Name: sky130_fd_pr__nfet_20v0_zvt

Operating Voltages where SPICE models are valid, subject to SOA limitations:

- $V_{DS} = 0$ to +22V
- $V_{GS} = 0$ to 5.5V
- $V_{BS} = 0$ to -2.0V

Details

The 20V NMOS zero-VT FET has p-well and all Vt implants blocked to achieve a zero VT.

Major model output parameters are shown below and compared against the EDR (e-test) specs

Param	W/L	Units	MODEL TT	FF	SS	FS	SF	EDR NOM	MIN	MAX
VTXNZVT1	2* 30/5.5	V	-0.03	-0.025	-0.024	-0.024	-0.025	-0.1224	-0.0228	-0.2228
VTBNZVT1	2* 30/5.5	V	-0.050	-0.061	0.095	0.095	-0.061	-0.0496	0.095	-0.1611
BVNZVT1	2* 30/5.5	V						48	30	80
IBBNZVT1	2* 30/5.5	µA/µm						0.033	0	0.1
ID5N0ZVT1	2* 30/5.5	mA	0.0279	0.1698	0.0035	0.0035	0.1698	0.0279	0.00354	0.1695
ID5NZVT1	2* 30/5.5	mA	1.376	1.854	0.850	0.850	1.854	1.368	0.8477	1.84
IDLN0ZVT1	2* 30/5.5	mA	0.0134	0.0689	0.0020	0.0020	0.0689	0.0134	0.00202	0.0688
IDLNZVT1	2* 30/5.5	mA	0.284	0.381	0.181	0.181	0.381	0.282	0.18	0.3777
IDSN0ZVT1	2* 30/5.5	mA	0.0336	0.2108	0.0044	0.0044	0.2108	0.0336	0.00447	0.2104
IDSNZVT1	2* 30/5.5	mA	12.85	17.50	8.35	8.35	17.50	12.79	8.366	17.38
RD-SNZVT1	2* 30/5.5	Ω	365.2	271.7	589.8	589.8	271.7	365.5	271.7	589.8
RSPONZVT1	2* 30/5.5	mΩ-mm^2	186.7	138.9	301.5	301.5	138.9	186.8	138.9	301.5
IOFFNZVT1	2* 30/5.5	LOG A	Max = -9.5	-11.57	-15	-9.706				

The symbol of the sky130_fd_pr__nfet_20v0_zvt (20V NMOS zero-VT FET) is still under development.

The cross-section of the 20V NMOS zero-VT FET is shown below.
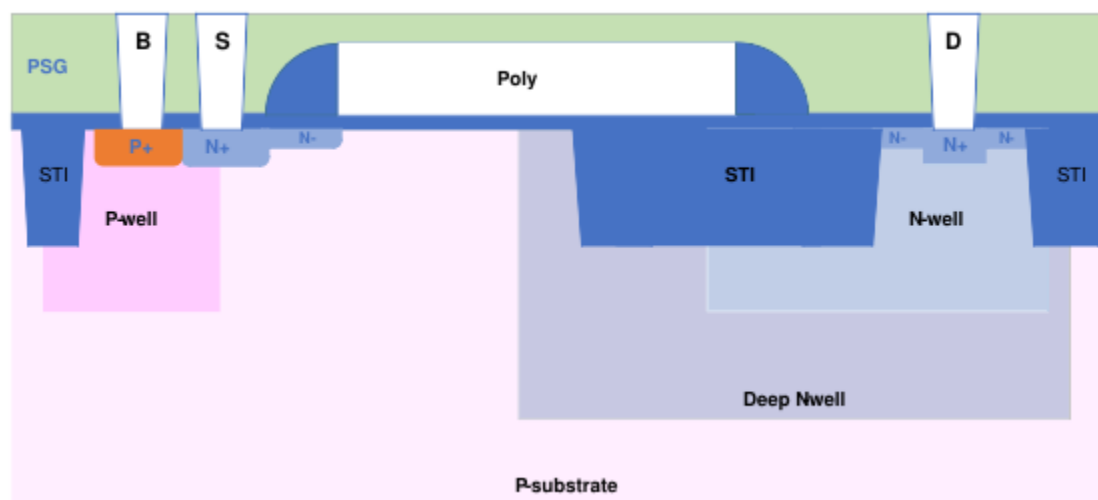
5.13.16 20V isolated NMOS FET

Spice Model Information

- Cell Name: sky130_fd_pr__nfet_extenddrain
- Model Name: sky130_fd_pr__nfet_20v0_iso

Operating Voltages where SPICE models are valid, subject to SOA limitations:

- $V_{DS} = 0$ to +22V
- $V_{GS} = 0$ to 5.5V
- $V_{BS} = 0$ to -2.0V

Details

The 20V isolated NMOS FET has the same construction as the 20V NMOS FET, but is built over a Deep N-well. This permits the p-well to be isolated from the substrate and permit "high-side" usage (where the PW body is held above ground).

Major model output parameters are shown below and compared against the EDR (e-test) specs

Param	W/L	Units	MODEL TT	FF	SS	FS	SF	EDR NOM	MIN	MAX
VTXN20VHVISO1	2* 30/1.0	V	0.817	0.637	0.998	0.998	0.637	0.8171	0.6372	0.9981
VTBN20VHVISO1	2* 30/1.0	V	1.817	1.567	2.069	2.069	1.567	1.817	1.567	2.069
BVN20VHVISO1	2* 30/1.0	V						29.78	26	40
IBB20N20VHVISO	2* 30/1.0	µA/µm						1.152	0	2
ID5N20VHVISO1	2* 30/1.0	mA	1.506	2.550	0.806	0.806	2.550	1.498	0.8033	2.526
IDLN20VHVISO1	2* 30/1.0	mA	0.336	0.578	0.174	0.174	0.578	0.3334	0.1732	0.5718
IDSN20VHVISO1	2* 30/1.0	mA	15.33	19.34	11.32	11.32	19.34	15.32	11.32	19.32
RDSP20VHVISO1	2* 30/1.0	Ω	333.7	197.9	622.4	622.4	197.9	333.7	197.9	622.4
RSPOP20VHVISO	2* 30/1.0	mΩ-mm^2	100.5	59.6	187.5	187.5	59.6	79.38	47.63	111.1
ILKN20VHVISO1	2* 30/1.0	LOG A	Max = -8.6	-	-18 11.58	- 8.162				

The symbol of the sky130_fd_pr__nfet_20v0_iso (20V isolated NMOS FET) is shown below.

The cross-section of the 20V isolated NMOS FET is shown below.

5.13.17 20V PMOS FET

Spice Model Information

- Cell Name: sky130_fd_pr__pfet_extenddrain
- Model Name: sky130_fd_pr__pfet_20v0

Operating Voltages where SPICE models are valid, subject to SOA limitations:

- $V_{DS} = 0$ to -22V
- $V_{GS} = 0$ to -5.5V
- $V_{BS} = 0$ to +2.0V

Details

The 20V NMOS FET has similar construction to the 11V/16V NMOS FET, with several differences:

- Longer drift region
- Longer poly gate
- Larger W/L
- Devices placed in pairs (drain in middle, sources on outside)

Major model output parameters are shown below and compared against the EDR (e-test) specs

Param	W/L	Units	MODEL TT	FF	SS	FS	SF	EDR NOM	MIN	MAX
VTXP20VHV1	2* 30/1.0	V	-1.043	- 0.843	- 1.243	- 1.243	- 0.843	- 1.043	- 1.243	- 0.843
VTBP20VHV1	2* 30/1.0	V	-1.588	- 1.331	- 1.845	- 1.331	- 1.845	- 1.588	- 1.845	- 1.331
BVP20VHV1	2* 30/1.0	V						36.31	28.00	60.00
ID5P20VHV1	2* 30/1.0	mA	1.292	1.818	0.772	0.772	1.818	1.286	0.7691	1.805
IDLP20VHV1	2* 30/1.0	mA	0.261	0.367	0.157	0.157	0.367	0.26	0.156	0.364
IDSP20VHV1	2* 30/1.0	mA	11.67	16.31	6.97	6.97	16.31	11.6	6.94	16.2
RDSP20VHV1	2* 30/1.0	Ω	388.9	277.0	650.1	650.1	277.0	388.9	277.0	650.1
RSPOP20VHV1	2* 30/1.0	$m\Omega\text{-}mm^2$	82.1	58.5	137.3	137.3	58.5	82.12	58.47	137.3
ILKP20VHV1	2* 30/1.0	LOG A	Max = - 8.9	- 11.63	-18	-9				

The symbol of the sky130_fd_pr__pfet_20v0 (20V PMOS FET) is shown below.
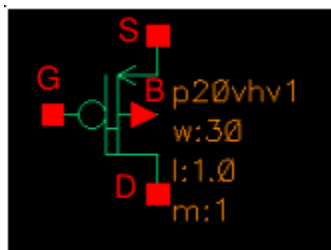
The cross-section of the 20V PMOS FET is shown below.
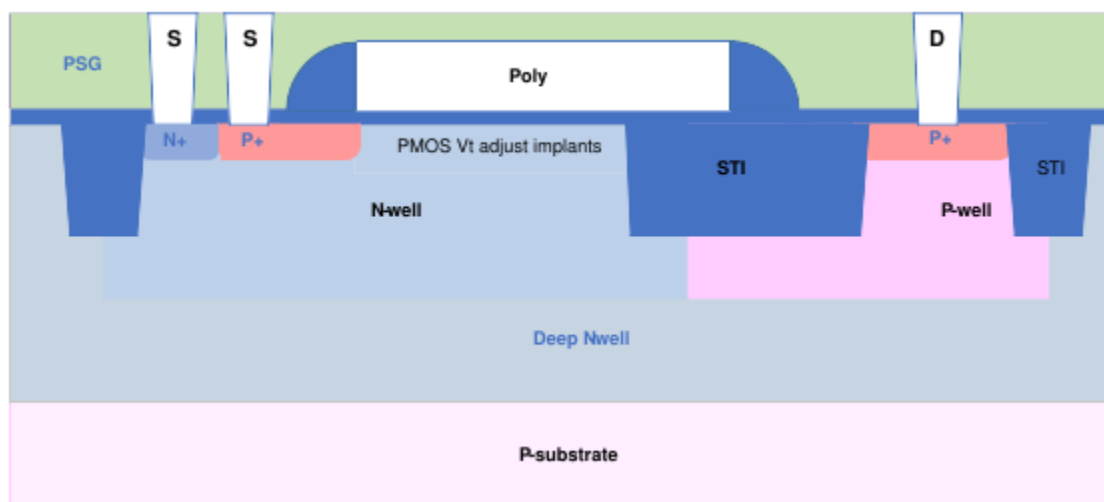
5.13.18 ESD NMOS FET

Spice Model Information

- Cell Name: sky130_fd_pr__nfet_01v8
- Model Name: sky130_fd_pr__esd_nfet_01v8, sky130_fd_pr__esd_nfet_g5v0d10v5, sky130_fd_pr__esd_nfet_g5v0d10v5_nvt

Operating Voltages where SPICE models are valid

- $V_{DS} = 0$ to 11.0V (sky130_fd_pr__nfet_g5v0d10v5*), 0 to 1.95V (sky130_fd_pr__nfet_01v8*)
- $V_{GS} = 0$ to 5.0V (sky130_fd_pr__nfet_g5v0d10v5*), 0 to 1.95V (sky130_fd_pr__nfet_01v8*)
- $V_{BS} = 0$ to -5.5V, (sky130_fd_pr__nfet_g5v0d10v5), +0.3 to -5.5V (sky130_fd_pr__nfet_05v0_nvt), 0 to -1.95V (sky130_fd_pr__nfet_01v8*)

Details

The ESD FET's differ from the regular NMOS devices in several aspects, most notably:

- Increased isolation spacing from contacts to surrounding STI
- Increased drain contact-to-gate spacing
- Placement of n-well under the drain contacts

Major model output parameters are shown below and compared against the EDR (e-test) specs

Param	W/L	Units	MODEL TT	FF	SS	FS	SF	EDR NOM	MIN	MAX
IDSNESD-HVS55	21.5/0.55	mA	12.172	13.073	11.277	13.144	11.207	11.46	10.57	12.35
ILKNESD-HVS55	21.5/0.55	LOG A	Max = -10.8	-12.49	-15	-11.21				
VTXNESD-HVS55	21.5/0.55	V	0.817	0.776	0.858	0.876	0.758	0.812	0.752	0.871
IDSNESDLVS	20.35/0.165	mA	9.954	11.027	8.877	11.055	8.84	8.145	7.216	9.075
ILKNESDLVS	20.35/0.165	LOG A	Max = -10.13	-10.85	-12.15	-10.15				
VTXNESDLVS	20.35/0.165	V	0.669	0.621	0.715	0.737	0.599	0.6416	0.5706	0.7125

The symbols of the sky130_fd_pr__esd_nfet_g5v0d10v5 and sky130_fd_pr__esd_nfet_g5v0d10v5_nvt (ESD NMOS FET) are shown below:
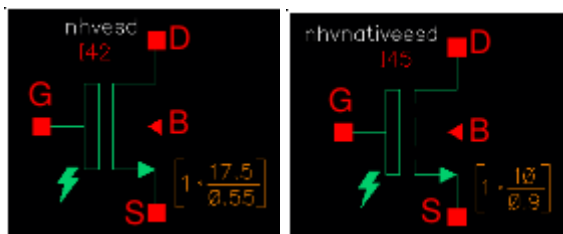
The cross-section of the ESD NMOS FET is shown below.
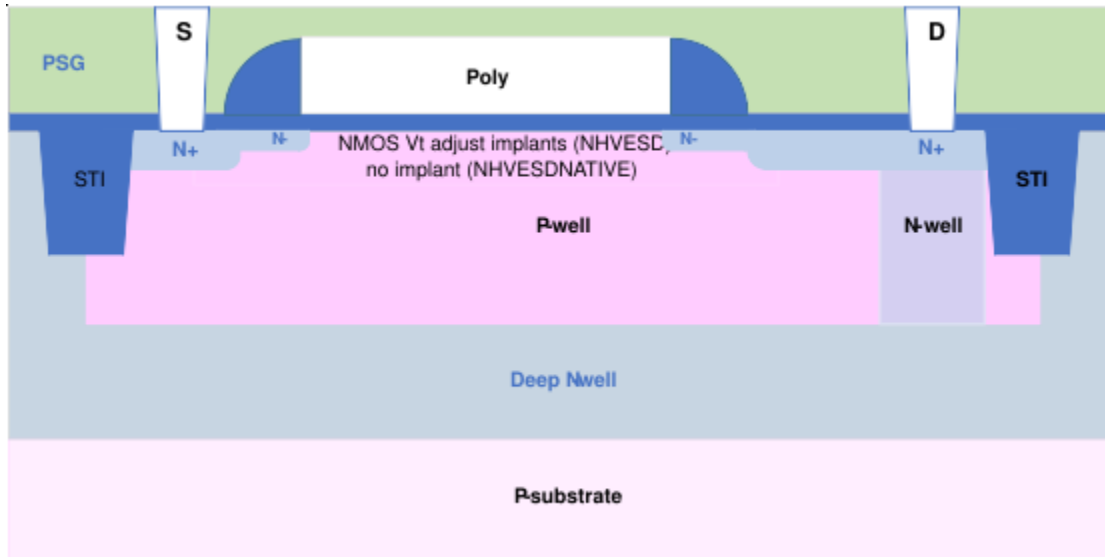
5.13.19 Diodes

Spice Model Information

- Cell Name: **:cell:`diode`**

- Model Names: sky130_fd_pr__diode_pw2nd_05v5, sky130_fd_pr__diode_pw2nd_11v0, sky130_fd_pr__diode_pw2nd_05v5_nvt, sky130_fd_pr__diode_pw2nd_05v5_lvt, sky130_fd_pr__diode_pd2nw_05v5, sky130_fd_pr__diode_pd2nw_11v0, sky130_fd_pr__diode_pd2nw_05v5_hvt, sky130_fd_pr__diode_pd2nw_05v5_lvt, sky130_fd_pr__model__parasitic__rf_diode_ps2nw, sky130_fd_pr__model__parasitic__rf_diode_pw2dn, sky130_fd_pr__model__parasitic__diode_pw2dn, sky130_fd_pr__model__parasitic__diode_ps2dn, **:model:`dnwdiode_psub_victim`**, **:model:`dnwdiode_psub_aggressor`**, sky130_fd_pr__model__parasitic__diode_ps2nw, **:model:`nwdiode_victim`**, **:model:`nwdiode_aggressor`**, **:model:`xesd_ndiode_h_X`**, **:model:`xesd_ndiode_h_dnwl_X`**, **:model:`xesd_pdiode_h_X (X = 100 or 200 or 300)`**

- Cell Name: **:cell:`lvsdiode`**

- Model Names: sky130_fd_pr__diode_pw2nd_05v5, sky130_fd_pr__diode_pw2nd_11v0, sky130_fd_pr__diode_pd2nw_05v5, sky130_fd_pr__diode_pd2nw_11v0, sky130_fd_pr__model__parasitic__diode_ps2dn, **:model:`dnwdiode_psub_victim`**, **:model:`dnwdiode_psub_aggressor`**, **:model:`nwdiode_victim`**, **:model:`nwdiode_aggressor`**, **:model:`xesd_ndiode_h_X`**, **:model:`xesd_ndiode_h_dnwl_X`**, **:model:`xesd_pdiode_h_X (X = 100 or 200 or 300)`**

Operating regime where SPICE models are valid

- $|V_{d0} \smile V_{d1}| = 0$ to 5.0V

Details

Parameter	NOM	LSL	USL	Units	Description
BVN	11.7	10.7	14.0	V	N+ breakdown voltage
BVNH	12.7	11.7	14.0	V	HV N+ breakdown voltage
BVNE	11	9.5	14.5	V	N+ peripheral breakdown voltage
BVNEH	12.2	11.5	14.5	V	HV N+ peripheral breakdown voltage
BVP	12.2	10.2	14.5	V	P+ breakdown voltage
BVPH	12	11.2	14.5	V	HV P+ breakdown voltage
BVPE	10.5	9	14.5	V	P+ peripheral breakdown voltage
BVPEH	11.6	11.2	14.5	V	HV P+ peripheral breakdown voltage

Symbols for the diodes are shown below

5.13.20 Bipolar NPN transistor

Spice Model Information

- Cell Name: sky130_fd_pr__npn_05v5

- Model Names: sky130_fd_pr__npn_05v5, sky130_fd_pr__npn_11v0

Operating regime where SPICE models are valid

- $|V_{CE}| = 0$ to 5.0V

- $|V_{BE}| = 0$ to 5.0V

- $I_{CE} = 0.01$ to 10 µA/µm^2

Details

The SKY130 process offers "free" NPN devices. The NPN uses the deep n-well as the collector. The device is not optimized, and must be used in the forward-active mode. The following sizes of NPN's are available:

- ungated device with emitter 1.0 x 1.0

- ungated device with emitter 1.0 x 2.0

- poly-gated version with octagonal emitter of A = 1.97 µm^2

The sky130_fd_pr__npn_11v0 device has a poly gate placed between the emitter and base diffusions, to prevent carrier recombination at the STI edge and increase β. The poly gate is connected to the emitter terminal.

Using this device must be done in conjunction with the correct guard rings, to avoid potential latchup issues with nearby circuitry. Reverse-active mode operation of the BJT's are neither modeled nor permitted. E-test specs for the NPN devices are shown in the table below:

Parameter	NOM	LSL	USL	Units	Description
BFNPN1X1_10P0	37.5	18.14	56.93		NPN forward Current Gain ($\frac{I_C}{I_B}$) at $I_E = 10A$
BFNPN1X1_1P0	36.72	17.97	55.38		NPN forward Current Gain ($\frac{I_C}{I_B}$) at $I_E = 1.0A$
BFNPN1X2_17P5	35.14	16.98	53.37		NPN forward Current Gain ($\frac{I_C}{I_B}$) at $I_E = 17.5A$
BFNPN1X2_1P75	34.57	16.89	52.2		NPN forward Current Gain ($\frac{I_C}{I_B}$) at $I_E = 1.75A$
BFNPNPOLY_3P16	125.28	62.37	500		NPN forward Current Gain ($\frac{I_C}{I_B}$) at $I_E = 3.16A$
BFNPNPOLY_P316	106.98	55.94	500		NPN forward Current Gain ($\frac{I_C}{I_B}$) at $I_E = 0.316A$
VBENPN1X1_10P0	0.7745	0.7645	0.7845	V	NPN emitter-base voltage at $I_E = 10A$
VBENPN1X1_1P0	0.712	0.702	0.722	V	NPN emitter-base voltage at $I_E = 1.0A$
VBENPN1X2_17P5	0.7745	0.7645	0.7845	V	NPN emitter-base voltage at $I_E = 17.5A$
VBENPN1X2_1P75	0.712	0.702	0.722	V	NPN emitter-base voltage at $I_E = 1.75A$
VBENPN-POLY_3P16	0.7073	0.6933	0.7213	V	NPN emitter-base voltage at $I_E = 3.16A$
VBENPN-POLY_P316	0.6452	0.6312	0.6591	V	NPN emitter-base voltage at $I_E = 0.316A$

Symbols for the sky130_fd_pr__npn_05v5 are shown below
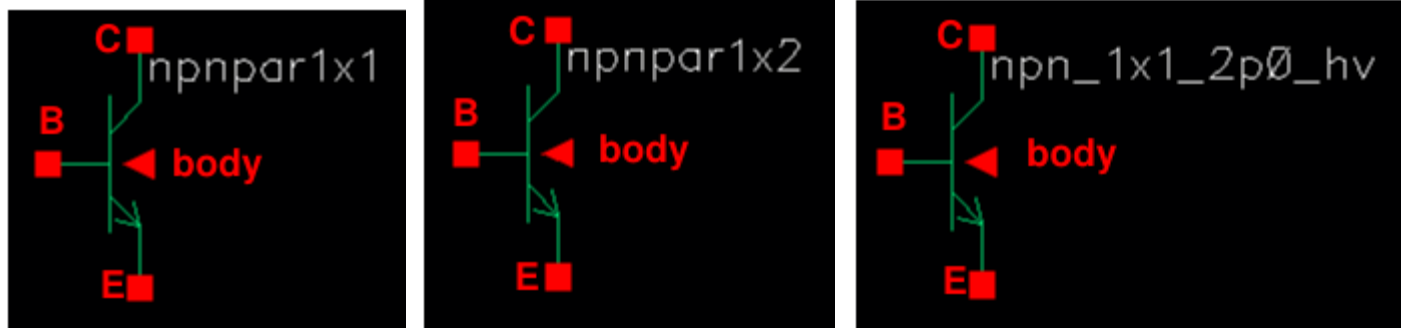
The cross-section of the sky130_fd_pr__npn_05v5 is shown below.
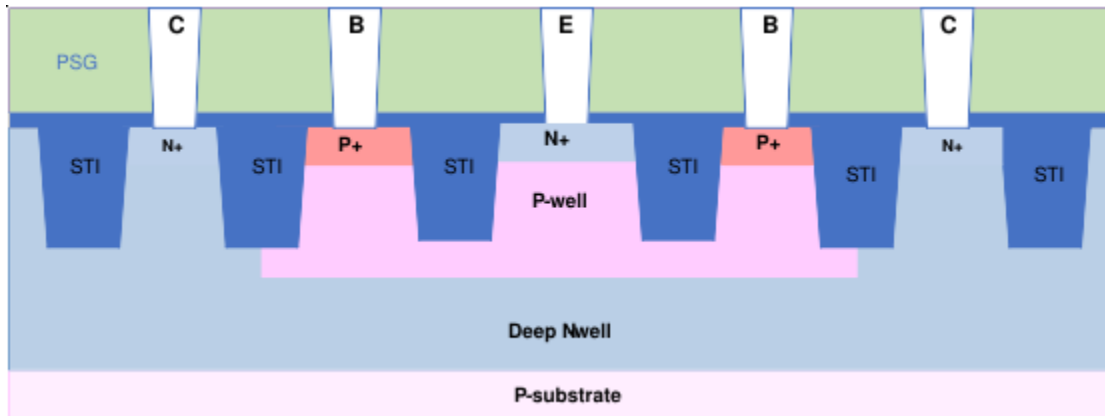
The cross-section of the sky130_fd_pr__npn_11v0 is shown below. The poly gate is tied to the emitter to prevent the parasitic MOSFET from turning on.
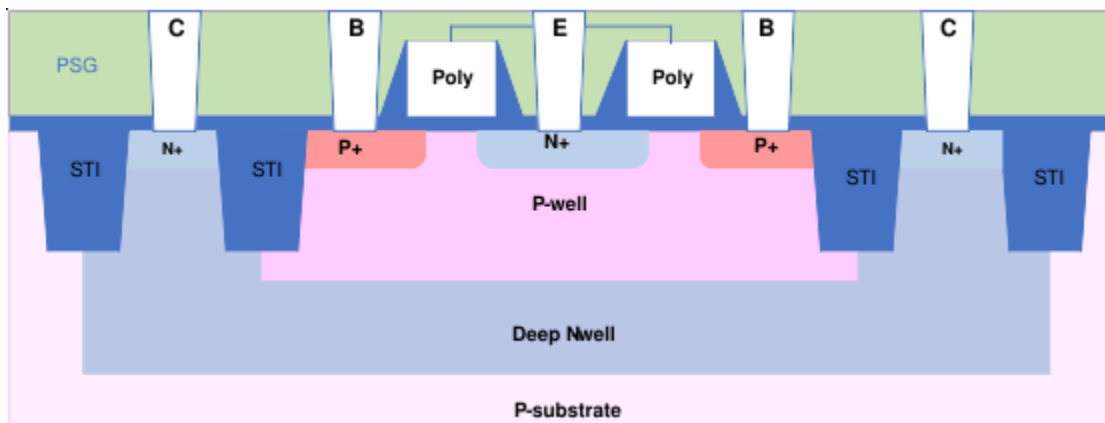
5.13.21 Bipolar PNP transistor

Spice Model Information

- Cell Name: sky130_fd_pr__pnp_05v5

- Model Names: sky130_fd_pr__pnp_05v5, sky130_fd_pr__pnp_05v5

Operating regime where SPICE models are valid

- $|V_{CE}| = 0$ to 5.0V

- $|V_{BE}| = 0$ to 5.0V

- $I_{CE} = 0.01$ to 10 μA/μm^2

Details

The SKY130 process offer a "free" PNP device, which utilizes the substrate as the collector. This device is not independently optimized, and can be used in forward-active mode. The following sizes of PNP are available:

- ungated device with emitter 0.68 x 0.68 (A=0.4624 μm^2)

- ungated device with emitter 3.4 x 3.4 (A=11.56 μm^2)

Using this device must be done in conjunction with the correct guard rings, to avoid potential latchup issues with nearby circuitry. Reverse-active mode operation of the BJT's are neither modeled nor permitted.

E-test specs for these devices are shown in the table below:

Parameter	NOM	LSL	USL	Units	Description
BF0P68_0P5	14.29	7.51	21.02		PNP forward current gain ($\frac{I_C}{I_B}$) at $I_E = 0.5A$
BF0P68_5	12.58	6.59	18.59		PNP forward current gain ($\frac{I_C}{I_B}$) at $I_E = 5.0A$
VBE0P68_0P5	0.7180	0.7120	0.7240	V	PNP emitter-base voltage at $I_E = 0.5A$
VBE0P68_5	0.7847	0.7790	0.7904	V	PNP emitter-base voltage at $I_E = 5.0A$
BF3P4_0P1	13.20	5.93	20.20		PNP forward current gain ($\frac{I_C}{I_B}$) at $I_E = 0.1A$
BF3P4_10	14.65	6.10	23.10		PNP forward current gain ($\frac{I_C}{I_B}$) at $I_E = 1.0A$
VBE3P4_0P1	0.6129	0.6087	0.6172	V	PNP emitter-base voltage at $I_E = 0.1A$
VBE3P4_10	0.7351	0.7308	0.7393	V	PNP emitter-base voltage at $I_E = 1.0A$

Symbols for the sky130_fd_pr__pnp_05v5 is shown below
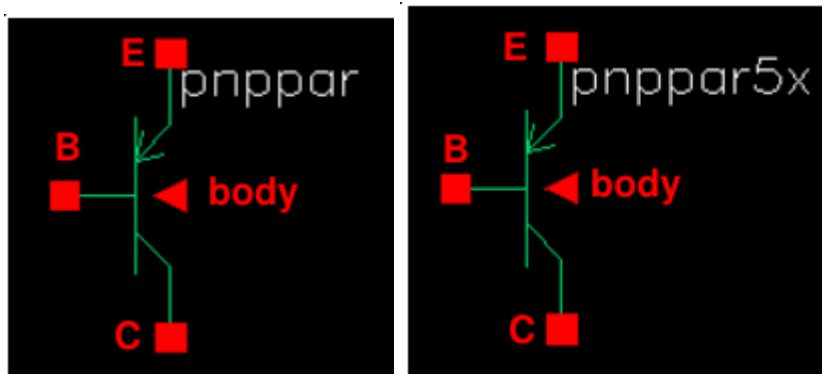
The cross-section of the sky130_fd_pr__pnp_05v5 is shown below.

No deep n-well exists in this device; the collector is the substrate.
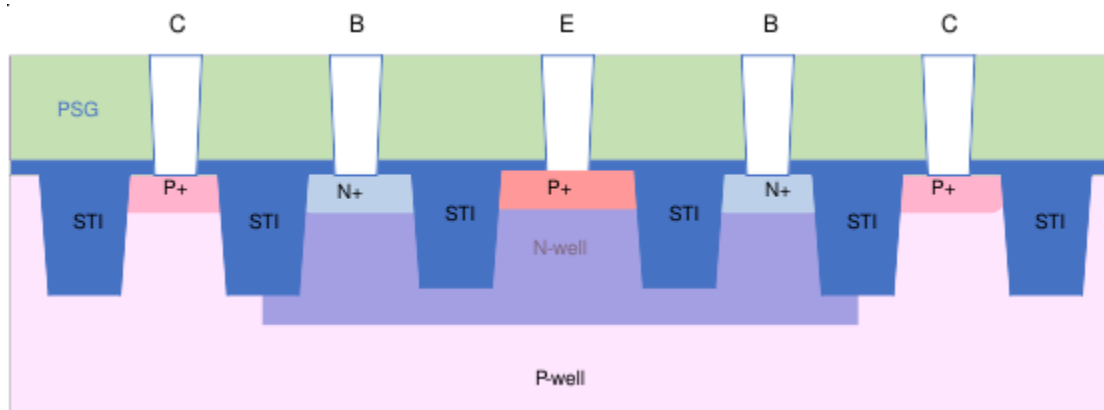
5.13.22 SRAM cells

The SKY130 process currently supports only single-port SRAM's, which are contained in hard-IP libraries. These cells are constructed with smaller design rules (Table 9), along with OPC (optical proximity correction) techniques, to achieve small memory cells. Use of the memory cells or their devices outside the specific IP is prohibited. The schematic for the SRAM is shown below in Figure 10. This cell is available in the S8 IP offerings and is monitored at e-test through the use of "pinned out" devices within the specific arrays.
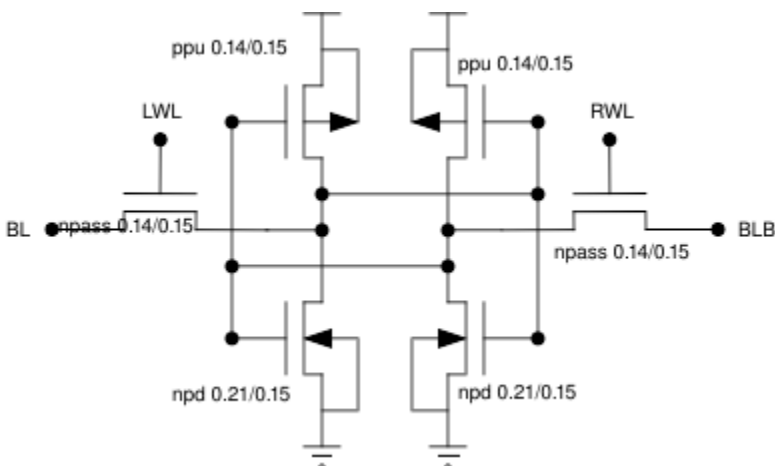
Figure 10. Schematics of the Single Port SRAM.

A Dual-Port SRAM is currently being designed using a similar approach. Compilers for the SP and DP SRAM's will be available end-2019.

Operating Voltages where SPICE models are valid

- $V_{DS} = 0$ to 1.8V

- $V_{GS} = 0$ to 1.8V

- $V_{BS} = 0$ to -1.8V

Details

N-pass FET (SRAM)

Spice Model Information

- Cell Name: sky130_fd_pr__nfet_01v8

- Model Name (SRAM): sky130_fd_pr__special_nfet_pass

Parameter	W/L	Units	MODEL					EDR		
			TT	FF	SS	FS	SF	NOM	MIN	MAX
VTXNPAS	0.14/0.15	V	0.68	0.52	0.846	0.846	0.515	0.669	0.498	0.839
IDSNPAS	0.14/0.15	µA	0.0702	0.0948	0.0471	0.0943	0.0473	68.2	45.5	90.8
ILKNPAS	0.14/0.15	LOG A	Max = -8.0	-9.73	-12.33	-9.1				

N-latch FET (SRAM)

Spice Model Information

- Cell Name: sky130_fd_pr__nfet_01v8

- Model Name (SRAM): sky130_fd_pr__special_nfet_latch

Parameter	W/L	Units	MODEL					EDR		
			TT	FF	SS	FS	SF	NOM	MIN	MAX
VTXNLTC	0.21/0.15	V	0.715	0.574	0.856	0.856	0.575	0.709	0.567	0.851
IDSNLTC	0.21/0.15	µA	0.091	0.1197	0.0616	0.1192	0.0618	87.9	60.2	115.5
ILKNLTC	0.21/0.15	LOG A	Max = -7.8	-9.45	-11.65	-8.90				

P-latch FET (SRAM)

Spice Model Information

- Cell Name: sky130_fd_pr__pfet_01v8

- Model Name (SRAM): sky130_fd_pr__special_pfet_pass

Parameter	W/L	Units	MODEL					EDR		
			TT	FF	SS	FS	SF	NOM	MIN	MAX
VTXPLTC	0.14/0.15	V	-0.918	-0.761	-1.085	-0.747	-1.089	-0.905	-1.080	-0.732
IDSPLTC	0.14/0.15	µA	0.0208	0.0306	0.0113	0.0304	0.0113	19.9	10.7	29.1
ILKPLTC	0.14/0.15	LOG A	Max = -7.3	-9.860	-13.31	-8.880				

5.13.23 SONOS cells

The SKY130 process currently supports two SONOS flash memory cells:

- The original cell is supported in the S8PFHD, S8PHRC and S8PFN-20 technology options, with operating temperatures from -55°C to +155°C

- The "star" cell is supported in the S8PHIRS technology option. Its cell size is approximately 25% smaller than the original cell, but its temperature range is restricted to -40°C to +125°C.

Spice models for the memory cells exist for multiple conditions:

MODEL CORNERS (*.cor)	Programmed	Erased
Beginning of Life	sonos_bol_p	sonos_bol_e
End of Life	sonos_eol_p	sonos_eol_e

Program and Erase characteristics are described in more detail in the ***S8 Nonvolatile Technology Spec*** (001-08712), and summarized below:

Condition	V_G	V_D	V_B	V_S	V_{WL}	Pulse
Read	0	+1.1	0	0	+1.8	n/a
Program	+6.7	-3.8	-3.8	-38	Float	2 ms
Erase	-3.8	+6.7	+6.7	+6.7	Float	6 ms
VT meas	$I_D = 2.05\mu A$	+1.1	0	0	+1.8	n/a

Endurance behavior is illustrated below (100K cycles guaranteed):

.
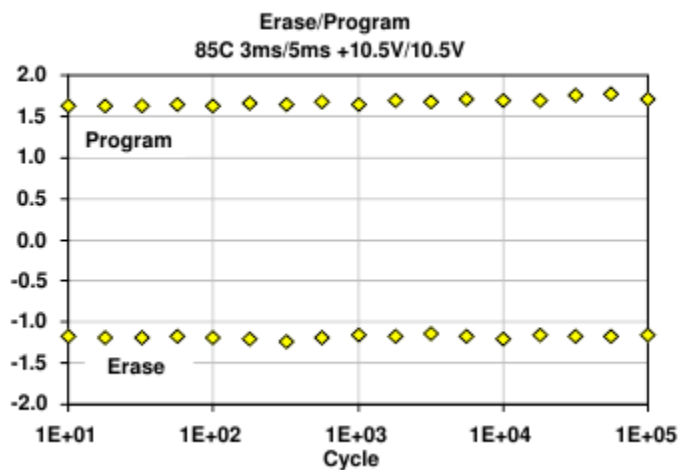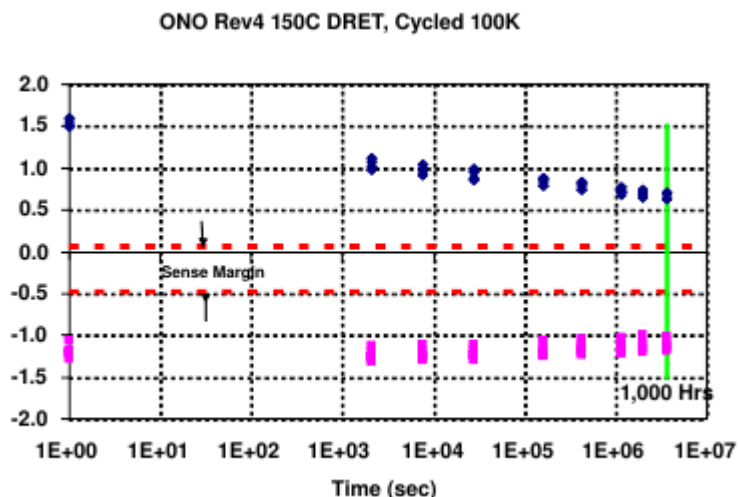
Data retention behavior is shown below at 85C

E-test parameters are summarized below for both original and star cells:

Parameter	W/L	NOM	LSL	USL	Units	Description
IDSE4522C	0.45/0.22	85	27	144	µA	SONOS erased current at Vwl=5.0
IDSE4522RC	0.45/0.22	46	20	72	µA	SONOS erased current at Vwl=1.8
IDSP4522RC	0.45/0.22	0.003	0	2	nA	SONOS programmed current at Vwl=1.8
IDSP4522RC_SP	0.45/0.22	0.003	0	0.074	nA	SONOS programmed current with Smart Program
IDSP14522RC	0.45/0.22	28	10	61.4	µA	SONOS program inhibit current, Vwl=1.8
ID-SPI4522C_SP	0.45/0.22	37	15.3	83.6	µA	SONOS program inhibit current, Vwl=5.0
VTE4522C	0.45/0.22	-2.3	-3.648	-0.952	V	SONOS erased VT (VG@2.05uA)
VTP4522C	0.45/0.22	1.44	0.672	2.472	V	SONOS programmed VT (VG@2.05uA)
VTP4522C_SP	0.45/0.22	1.44	1.172	1.972	V	SONOS programmed VT with Smart Program
VTPI4522C	0.45/0.22	-1.132	-2.055	-0.512	V	SONOS program inhibit VT (VG@2.05uA)
VTPI4522C_SP	0.45/0.22	-1.132	-2.055	-0.512	V	SONOS program inhibit VT, Smart Program
IDSE3515C	0.35/0.15	0.0518	0.0162	0.103	mA	SONOS erased current at Vwl=5.0
IDSE3515RC	0.35/0.15	0.03	0.0128	0.049	mA	SONOS erased current at Vwl=1.8
IDSP3515RC	0.35/0.15	0.015	0	32	nA	SONOS programmed current at Vwl=1.8
IDSP3515RC_SP	0.35/0.15	0.015	0.001	0.172	nA	SONOS programmed current with Smart Program
IDSP13515RC	0.35/0.15	0.032	0.0089	0.0602	mA	SONOS program inhibit current, Vwl=1.8
ID-SPI3515C_SP	0.35/0.15	0.032	0.0153	0.0551	mA	SONOS program inhibit current, Vwl=5.0
VTE3515C	0.35/0.15	-1.91	-3.26	-0.71	V	SONOS erased VT (VG@2.05uA)
VTP3515C	0.35/0.15	1.44	0.49	2.472	V	SONOS programmed VT (VG@2.05uA)
VTP3515C_SP	0.35/0.15	1.44	1.172	1.972	V	SONOS programmed VT with Smart Program
VTPI3515C	0.35/0.15	-1.235	-2.158	-0.415	V	SONOS program inhibit VT (VG@2.05uA)
VTPI3515C_SP	0.35/0.15	-1.235	-1.965	-0.675	V	SONOS program inhibit VT, Smart Program

The schematic for the 2-T SONOS memory cell is shown below:
.

The cross-section of the 2-T SONOS cell is shown below.
.
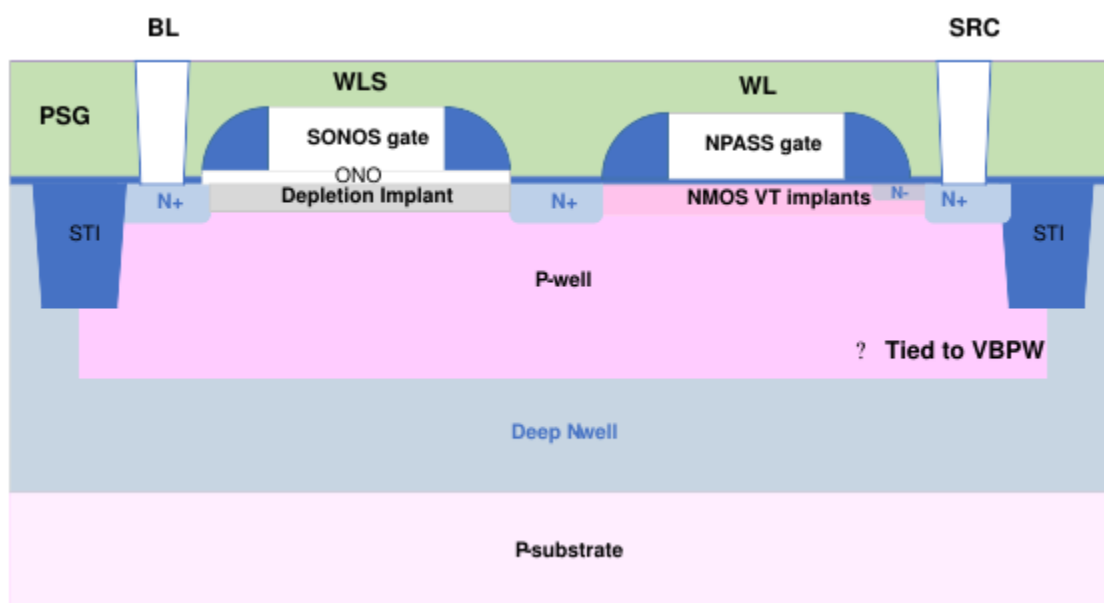
5.13.24 Generic resistors

Generic resistors are supported in the PDK but are not recommended for analog applications. Resistor values will be extracted from the layout as long as the resistor layer is utilized, for LVS against schematic elements.

The following 3-terminal resistors are available, and have built-in diodes inside the models:

- N+ diffusion (type " sky130_fd_pr__res_generic_nd ", model sky130_fd_pr__res_generic_nd)
- P+ diffusion (type " sky130_fd_pr__res_generic_pd ", model sky130_fd_pr__res_generic_pd)
- P-well (type "sky130_fd_pr__res_generic_pw", model sky130_fd_pr__res_iso_pw)

The following 2-terminal resistors are available:

- N+ doped gate poly (sky130_fd_pr__res_generic_po)
- Local interconnect (sky130_fd_pr__res_generic_l1)
- Metal-1 (sky130_fd_pr__res_generic_m1)
- Metal-2 (sky130_fd_pr__res_generic_m2)

- Metal-3 (sky130_fd_pr__res_generic_m3)
- Metal-4 (sky130_fd_pr__res_generic_m4)
- Metal-5 (sky130_fd_pr__res_generic_m5)

Specs for the generic resistors are shown below.

Parameter	NOM	LSL	USL	Units	Description
RSN	120	108	132	Ω/□	N+ diffusion sheet resistance
RSNH	114	102	126	Ω/□	HV N+ diffusion sheet resistance
RSNW	950	550	1350	Ω/□	N-Well sheet resistance
RSP	197	166	228	Ω/□	P+ diffusion sheet resistance
RSPH	191	160	228	Ω/□	HV P+ diffusion sheet resistance
RSPW	3050	2565	3535	Ω/□	P-Well sheet resistance
RSDNW	2200	1825	2575	Ω/□	Deep N-Well sheet resistance
WN	0.157	0.088	0.226	μm	Electrical N+ linewidth (drawn 0.14)
WP	0.144	0.084	0.204	μm	Electrical P+ linewidth (drawn 0.14)
RSGPVDP	48.2	42.2	55.8	Ω/□	poly sheet resistance, with NGNIT
WGPUC15	0.094	0.053	0.135	μm	Electrical poly linewidth (drawn 0.15)
RSLI	12.8	9.2	17.0	Ω/□	Local interconnect sheet resistance
RSM1	0.125	0.105	0.145	Ω/□	Metal-1 sheet resistance
RSM2	0.125	0.105	0.145	Ω/□	Metal-2 sheet resistance
RSM3	0.047	0.038	0.056	Ω/□	Metal-3 sheet resistance
RSM4	0.047	0.038	0.056	Ω/□	Metal-4 sheet resistance
RSM5	0.0285	0.0212	0.0358	Ω/□	Metal-5 sheet resistance

Symbols for all resistors are shown below:
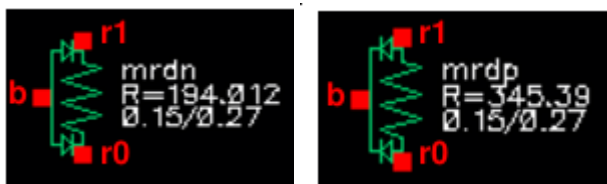
sky130_fd_pr__res_generic_nd sky130_fd_pr__res_generic_pd

sky130_fd_pr__res_generic_pw sky130_fd_pr__res_generic_po

sky130_fd_pr__res_generic_l1 sky130_fd_pr__res_generic_m1

sky130_fd_pr__res_generic_m2 sky130_fd_pr__res_generic_m3

sky130_fd_pr__res_generic_m4 sky130_fd_pr__res_generic_m5

5.13.25 P+ poly precision resistors

Spice Model Information

- Cell Name: **:cell:`res_high_po_XpXX`**, sky130_fd_pr__res_high_po
- Model Type: subcircuit

Operating ranges where SPICE models are valid

- $|V_{r0}\check{\ }V_{r1}| = 0$ to 5.0V
- Currents up to 500 µA/µm of width (preferred use ≤ 100 µA/µm)

Details

The resistors have 5 different fixed widths, plus a variable W/L option.

- 0.35 (0p35)
- 0.69 (0p69)
- 1.41 (1p41)
- 2.85 (2p83)
- 5.73 (5p73)

They are modeled as subcircuits, using a conventional resistor model combined with the capacitance under the resistor, as well as matching parameters and temperature coefficients. The fixed-width resistors may only be used in the above configurations. Each resistor end is contacted using a slot licon. Length is variable and measured between the front ends of the slot licons.

The fixed-width resistors are modeled using the equation

*R_0***** = head/tail resistance [Ω] (dominated by the slot licons)

*R_1***** = body resistance [Ω/µm] = R_{SH}/W

A top-down schematic drawing of the precision resistor is shown below.
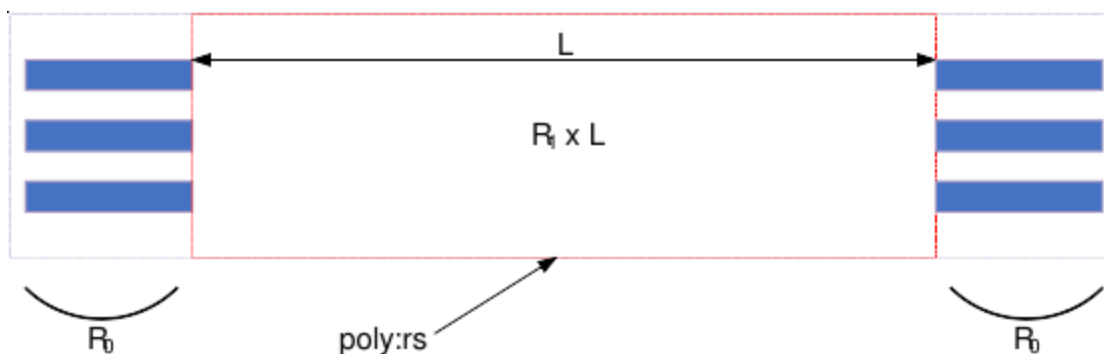
In addition to the R_0 and R_1 values, several fixed-value resistors are measured at e-test, as shown in the table below:

Parameter	NOM	LSL	USL	Units	Description
RP0P35X1SQ	964.2	593.5	1335	Ω	P+ poly resistor, 0.35 µm wide, 1 square
RP0P35X2SQ	1326	944.1	1708	Ω	P+ poly resistor, 0.35 µm wide, 2 squares
RP0P35X4SQ	2054	1624	2484	Ω	P+ poly resistor, 0.35 µm wide, 4 squares
RP0P35X20SQ	7888	6691	9086	Ω	P+ poly resistor, 0.35 µm wide, 20 squares
RP0P69NONLIN	30	25	35	%	P+ poly resistor non-linearity
RP0P69XP5SQ	575.3	366.8	783.8	Ω	P+ poly resistor, 0.69 µm wide, 0.5 square
RP0P69X1SQ	738	528	948.1	Ω	P+ poly resistor, 0.69 µm wide, 1 square
RP0P69X2SQ	1075	846.2	1303	Ω	P+ poly resistor, 0.69 µm wide, 2 squares
RP0P69X4SQ	1754	1458	2050	Ω	P+ poly resistor, 0.69 µm wide, 4 squares
RP0P69X20SQ	7201	6095	8307	Ω	P+ poly resistor, 0.69 µm wide, 20 squares
RP1P41XP5SQ	428.9	312.1	545.6	Ω	P+ poly resistor, 1.41 µm wide, 0.5 square
RP1P41X1SQ	585.9	463.8	708	Ω	P+ poly resistor, 1.41 µm wide, 1 square
RP1P41X2SQ	908.5	760.4	1057	Ω	P+ poly resistor, 1.41 µm wide, 2 squares
RP1P41X4SQ	1558	1332	1784	Ω	P+ poly resistor, 1.41 µm wide, 4 squares
RP1P41X20SQ	6764	5774	7754	Ω	P+ poly resistor, 1.41 µm wide, 20 squares
RP2P83XP5SQ	296.8	232.2	361.3	Ω	P+ poly resistor, 2.83 µm wide, 0.5 square
RP2P83X1SQ	457.1	381.5	532.8	Ω	P+ poly resistor, 2.83 µm wide, 1 square
RP2P83X2SQ	780.9	669.9	891.9	Ω	P+ poly resistor, 2.83 µm wide, 2 squares
RP2P83X4SQ	1430	1233	1627	Ω	P+ poly resistor, 2.83 µm wide, 4 squares
RP2P83X20SQ	6626	5683	7568	Ω	P+ poly resistor, 2.83 µm wide, 20 squares
RP5P73XP5SQ	236.1	195.4	276.7	Ω	P+ poly resistor, 5.73 µm wide, 0.5 square
RP5P73X1SQ	395.3	339	451.7	Ω	P+ poly resistor, 5.73 µm wide, 1 square
RP5P73X2SQ	718.2	620.9	815.6	Ω	P+ poly resistor, 5.73 µm wide, 2 squares
RP5P73X4SQ	1366	1180	1553	Ω	P+ poly resistor, 5.73 µm wide, 4 squares
RP5P73X20SQ	6556	5636	7475	Ω	P+ poly resistor, 5.73 µm wide, 20 squares

More details on the use of the precision resistors, and their models, are in the document ***SKY130 process Family Device Models*** (002-21997), which can be obtained from SkyWater upon request.

The symbols for the 300 ohm/sq precision resistors are shown below:

sky130_fd_pr__res_high_po_0p35 sky130_fd_pr__res_high_po_0p69

sky130_fd_pr__res_high_po_1p41 sky130_fd_pr__res_high_po_2p85
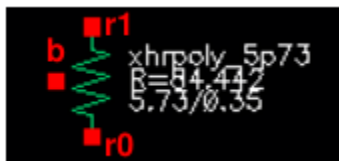
sky130_fd_pr__res_high_po_5p73

A generic version of the poly resistor is also available, which permits user inputs for W and L, and connections in series or parallel.

5.13.26 P- poly precision resistors

Spice Model Information

- Cell Name: **:cell:`res_xhigh_po_XpXX`**, sky130_fd_pr__res_xhigh_po
- Model Type: subcircuit

Operating ranges where SPICE models are valid

- $|V_{r0}\check{\ }V_{r1}| = 0$ to 5.0V
- Currents up to 500 µA/µm of width (preferred use ≤ 100 µA/µm)

Details

The resistors have 5 different fixed widths, plus a variable W/L option.

- 0.35 (0p35)
- 0.69 (0p69)
- 1.41 (1p41)
- 2.85 (2p83)
- 5.73 (5p73)

They are modeled as subcircuits, using a conventional resistor model combined with the capacitance under the resistor, as well as matching parameters and temperature coefficients. The fixed-width resistors may only be used in the above configurations. Each resistor end is contacted using a slot licon. Length is variable and measured between the front ends of the slot licons.

The resistors are modeled using the same equations as for the P+ poly resistors. In the case of the P- poly resistors, a separate implant is used to set the sheet resistance to 2000 ohm/sq.

Fixed value resistors have the same layout footprints as their P+ poly counterparts. Electrical and e-test specs are still TBD, once sufficient silicon has been evaluated. More details on the use of the precision resistors, and their models, are in the document ***SKY130 process Family Device Models*** (002-21997), currently under development.

The symbols for the 2000 ohm/sq precision resistors are shown below:

sky130_fd_pr__res_xhigh_po_0p35 sky130_fd_pr__res_xhigh_po_0p69

sky130_fd_pr__res_xhigh_po_1p41 sky130_fd_pr__res_xhigh_po_2p85
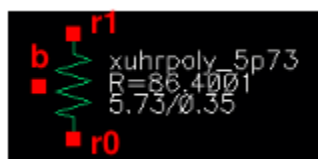
sky130_fd_pr__res_xhigh_po_5p73

A generic version of the poly resistor is also available, which permits user inputs for W and L, and connections in series or parallel.

5.13.27 MiM capacitors

Spice Model Information

- Cell Name: sky130_fd_pr__cap_mim_m3__base, sky130_fd_pr__cap_mim_m4__base
- Model Names: sky130_fd_pr__model__cap_mim, sky130_fd_pr__cap_mim_m4

Operating Voltages where SPICE models are valid

- $|V_{c0} \check{} V_{c1}| = 0$ to 5.0V

Details

The MiM capacitor is constructed using a thin dielectric over metal, followed by a thin conductor layer on top of the dielectric. There are two possible constructions:

- CAPM over Metal-3
- CAP2M over Metal-4

The constructions are identical, and the capacitors may be stacked to maximize total capacitance.

Electrical specs are listed below:

Parameter	NOM	LSL	USL	Units	Description
CMIMA	2	1.8	2.2	fF/μm^2	MiM cap area capacitance
CMIMP	0.19	0.11	0.27	fF/μm	MiM cap periphery capacitance
RSCAPM	5.8	4.8	6.8	Ω/□	MiM top plate sheet resistance
CMIM2A	2	1.8	2.2	fF/μm^2	MiM2 cap area capacitance
CMIM2P	0.19	0.11	0.27	fF/μm	MiM2 cap periphery capacitance
RSCAPM	5.8	4.8	6.8	Ω/sq	MiM2 top plate sheet resistance

The symbol for the MiM capacitor is shown below. Note that the cap model is a sub-circuit which accounts for the parasitic contact resistance and the parasitic capacitance from the bottom plate to substrate.
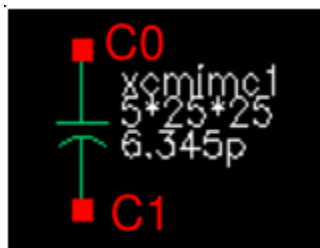
Cell name

M * W * L

Calc capacitance

The cross-section of the "stacked" MiM capacitor is shown below:
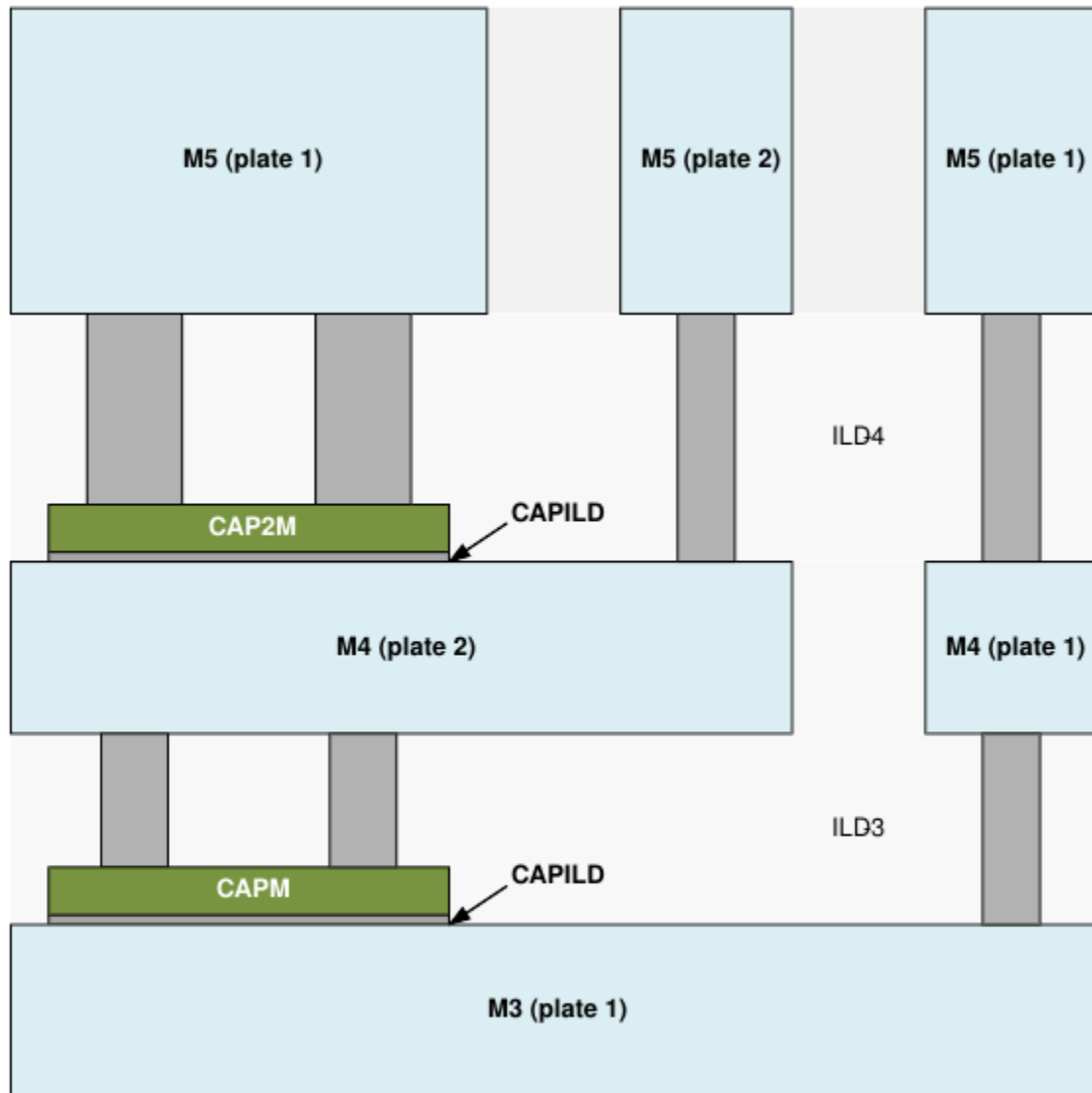
5.13.28 Vertical Parallel Plate (VPP) capacitors

Spice Model Information

- Cell Name: sky130_fd_pr__cap_vpp_XXpXxYYpY_{MM}(_shield(SS)*)(_float(FF)*)(_(VVVV))
- Model Names: sky130_fd_pr__cap_vpp_*
    - X and Y are size dimentions
    - MM refers to the layers which are used for the capacitance
    - SS refers to the layers which are used as shields (*noshield* when no shield is used)
    - FF refers to the layers which are floating.
    - VVVVV refers to the "variant" when there are multiple devices of the same configuration

Operating Voltages where SPICE models are valid

- $|V_{c0} \check{} V_{c1}| = 0$ to 5.5V

Details

The VPP caps utilize the tight spacings of the metal lines to create capacitors using the available metal layers. The fingers go in opposite directions to minimize alignment-related variability, and the capacitor sits on field oxide to minimize silicon capacitance effects. A schematic diagram of the layout is shown below:

Todo: M3

M2

LI

M1

LAYOUT of M2, M3, M4

LAYOUT of LI and M1 (with POLY sheet)

POLY

M4

These capacitors are fixed-size, and they can be connected together to multiply the effective capacitance of a given node. There are two different constructions.

Parallel VPP Capacitors

These are older versions, where stacked metal lines run parallel:

- sky130_fd_pr__cap_vpp_08p6x07p8_m1m2_noshield (M1 ∥ M2 only, 7.84 x 8.58)
- sky130_fd_pr__cap_vpp_04p4x04p6_m1m2_noshield_o2 (M1 ∥ M2 only, 4.38 x 4.59)
- sky130_fd_pr__cap_vpp_02p4x04p6_m1m2_noshield (M1 ∥ M2 only, 2.19 x 4.59)
- sky130_fd_pr__cap_vpp_04p4x04p6_m1m2_noshield (M1 ⊥ M2, 4.4 x 4.6, 4 quadrants)
- sky130_fd_pr__cap_vpp_11p5x11p7_m1m2_noshield (M1 ⊥ M2, 11.5 x 11.7, 4 quadrants)

- sky130_fd_pr__cap_vpp_44p7x23p1_pol1m1m2m3m4m5_noshield

- sky130_fd_pr__cap_vpp_02p7x06p1_m1m2m3m4_shieldl1_fingercap (M1 || M2 || M3 || M4, 2.7 x 5.0)

- sky130_fd_pr__cap_vpp_02p9x06p1_m1m2m3m4_shieldl1_fingercap2 (M1 || M2 || M3 || M4, 2.85 x 5.0)

- sky130_fd_pr__cap_vpp_02p7x11p1_m1m2m3m4_shieldl1_fingercap (M1 || M2 || M3 || M4, 2.7 x 10.0)

- sky130_fd_pr__cap_vpp_02p7x21p1_m1m2m3m4_shieldl1_fingercap (M1 || M2 || M3 || M4, 2.7 x 20.0)

- sky130_fd_pr__cap_vpp_02p7x41p1_m1m2m3m4_shieldl1_fingercap (M1 || M2 || M3 || M4, 2.7 x 40.0)

The symbol for these capacitors is shown below. The terminals c0 and c1 represent the two sides of the capacitor, with b as the body (sub or well).

Perpendicular VPP Capacitors

These are newer versions, where stacked metal lines run perpendicular and there are shields on top and bottom:

- sky130_fd_pr__cap_vpp_11p5x11p7_l1m1m2m3m4_shieldm5 (11.5x11.7, with M5 shield)

- sky130_fd_pr__cap_vpp_11p5x11p7_l1m1m2m3m4_shieldpom5 (11.5x11.7, with poly and M5 shield)

- sky130_fd_pr__cap_vpp_11p5x11p7_m1m2m3m4_shieldl1m5 (11.5x11.7, with LI and M5 shield)

- sky130_fd_pr__cap_vpp_04p4x04p6_m1m2m3_shieldl1m5_floatm4 (4.4x4.6, M3 float, LI / M5 shield)

- sky130_fd_pr__cap_vpp_08p6x07p8_m1m2m3_shieldl1m5_floatm4 (8.6x7.9, M3 float, LI / M5 shield)

- sky130_fd_pr__cap_vpp_11p5x11p7_m1m2m3_shieldl1m5_floatm4 (11.5x11.7, M3 float, LI / M5 shield)

- sky130_fd_pr__cap_vpp_11p5x11p7_l1m1m2m3_shieldm4 (11.5x11.7, with M4 shield)

- sky130_fd_pr__cap_vpp_06p8x06p1_l1m1m2m3_shieldpom4 (6.8x6.1, with poly and M4 shield)

- sky130_fd_pr__cap_vpp_06p8x06p1_m1m2m3_shieldl1m4 (6.8x6.1, with LI and M4 shield)

- sky130_fd_pr__cap_vpp_11p3x11p8_l1m1m2m3m4_shieldm5 (11.5x11.7, over 2 sky130_fd_pr__nfet_05v0_nvt of 10/4 each)

The symbol for these capacitors is shown below. The terminals c0 and c1 are the two capacitor terminals, "top" represents the top shield and "sub" the bottom shield.
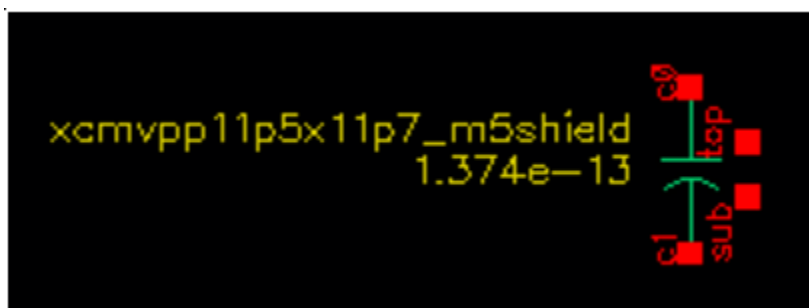
The capacitors are fixed-size elements and must be used as-is; they can be used in multiples.

Parameter	NOM	LSL	USL	Units	Description
CGGIVPPNA-TIVE	340.9	310.8	386	fF/cell	sky130_fd_pr__cap_vpp_11p3x11p8_l1m1m2m3m4_shieldm5_nhv, in inversion
VPP100LISM1M2	96.99	82.92	111.05	fF/cell	sky130_fd_pr__cap_vpp_11p5x11p7_m1m2m3_shieldl1
VPP100M1M2	74.6	57.82	91.39	fF/cell	sky130_fd_pr__cap_vpp_11p5x11p7_m1m2_noshield
VPP100M1M4M5	108.4	92.79	124	fF/cell	sky130_fd_pr__cap_vpp_11p5x11p7_m1m2m3m4_shieldm5
VPP12LISM1M2M	10.69	8.29	13.1	fF/cell	sky130_fd_pr__cap_vpp_04p4x04p6_m1m2m3_shieldl1
VPP12M1M2	7.81	6.05	9.57	fF/cell	sky130_fd_pr__cap_vpp_04p4x04p6_m1m2_noshield
VPP1LIM1M2	0.78	0.62	0.95	fF/cell	sky130_fd_pr__cap_vpp_01p8x01p8_m1m2_noshield
VPP25PYSM1M4	42.11	TBD	TBD	fF/cell	sky130_fd_pr__cap_vpp_06p8x06p1_l1m1m2m3m4_shieldpo_floatm5
VPP50LISM123M	42.75	33.35	50.87	fF/cell	sky130_fd_pr__cap_vpp_08p6x07p8_m1m2m3_shieldl1m5_floatm4
VPP50LISM1M2M	TBD	34.63	50.87	fF/cell	sky130_fd_pr__cap_vpp_08p6x07p8_m1m2m3_shieldl1
VPPSYM3	35	24.5	45.5	fF/cell	sky130_fd_pr__cap_vpp_08p6x07p8_m1m2_noshield
VPPSYM4	9.48	6.64	12.32	fF/cell	xcmppp4
VPPSYM5	4.37	3.06	5.68	fF/cell	sky130_fd_pr__cap_vpp_02p4x04p6_m1m2_noshield
VPP_100_LIM5S	116.75	99.94	133.56	fF/cell	sky130_fd_pr__cap_vpp_11p5x11p7_m1m2m3m4_shieldl1m5
VPP_100_M3S	97.56	84.63	110.79	fF/cell	sky130_fd_pr__cap_vpp_11p5x11p7_l1m1m2_shieldpom3
VPP_100_M4S	118.5	94.82	142.2	fF/cell	sky130_fd_pr__cap_vpp_11p5x11p7_l1m1m2m3_shieldm4
VPP_100_M5S	137.45	117.66	157.24	fF/cell	sky130_fd_pr__cap_vpp_11p5x11p7_l1m1m2m3m4_shieldm5
VPP_100_POLYM	121.9	97.51	146.3	fF/cell	sky130_fd_pr__cap_vpp_11p5x11p7_l1m1m2m3_shieldpom4
VPP_100_POLYM	141.23	120.89	161.57	fF/cell	sky130_fd_pr__cap_vpp_11p5x11p7_l1m1m2m3m4_shieldpom5

5.14 Error Messages

The `messages.csv file` provides a raw description for many of the automated DRC rules that are checked by Sky-Water as part of the acceptance criteria for GDS data.

Table 5.96: Table - Error Messages

ID	Name	Description
r0	x.1b	off 0.005 grid nwell vertex
r1	x.1b	off 0.005 grid diff vertex
r2	x.1b	off 0.005 grid dnwell vertex
r3	x.1b	off 0.005 grid tap vertex
r4	x.1b	off 0.005 grid lvtn vertex
r5	x.1b	off 0.005 grid hvtp vertex
r6	x.1b	off 0.005 grid hvi vertex
r7	x.1b	off 0.005 grid tunm vertex
r8	x.1b	off 0.005 grid poly vertex
r9	x.1b	off 0.005 grid npc vertex
r10	x.1b	off 0.005 grid nsdm vertex
r11	x.1b	off 0.005 grid psdm vertex
r12	x.1b	off 0.005 grid licon1 vertex
r13	x.1b	off 0.005 grid li1 vertex
r14	x.1b	off 0.005 grid mcon vertex
r15	x.1b	off 0.005 grid met1 vertex
r16	x.1b	off 0.005 grid via vertex
r17	x.1b	off 0.005 grid met2 vertex

continues on next page

Table 5.96 – continued from previous page

ID	Name	Description
r18	x.1b	off 0.005 grid vhvi vertex
r19	x.1b	off 0.005 grid via2 vertex
r20	x.1b	off 0.005 grid met3 vertex
r21	x.1b	off 0.005 grid via3 vertex
r22	x.1b	off 0.005 grid met4 vertex
r23	x.1b	off 0.005 grid via4 vertex
r24	x.1b	off 0.005 grid met5 vertex
r25	x.1b	off 0.005 grid nsm vertex
r26	x.1b	off 0.005 grid pad vertex
r27	x.1b	off 0.005 grid ldntm vertex
r28	x.1b	off 0.005 grid hvntm vertex
r29	x.1b	off 0.005 grid pnp vertex
r30	x.1b	off 0.005 grid capacitor vertex
r31	x.1b	off 0.005 grid ncm vertex
r32	x.1b	off 0.005 grid inductor vertex
r33	x.1b	off 0.005 grid rpm vertex
r34	x.1b	off 0.005 grid hvtr vertex
r35	x.1b	off 0.005 grid metop1 vertex
r36	x.1b	off 0.005 grid metop2 vertex
r37	x.1b	off 0.005 grid metop3 vertex
r38	x.1b	off 0.005 grid metop4 vertex
r39	x.1b	off 0.005 grid metop5 vertex
r40	x.1b	off 0.005 grid metop6 vertex
r41	x.1b	off 0.005 grid metop7 vertex
r42	x.1b	off 0.005 grid metop8 vertex
r43	x.1b	off 0.005 grid NTMdrop vertex
r44	x.1b	off 0.005 grid LVTNMdrop vertex
r45	x.1b	off 0.005 grid HVTPMdrop vertex
r46	x.1b	off 0.005 grid LI1Mdrop vertex
r47	x.1b	off 0.005 grid LICM1drop vertex
r48	x.1b	off 0.005 grid PSDMdrop vertex
r49	x.1b	off 0.005 grid NSDMdrop vertex
r50	x.1b	off 0.005 grid FOMdrop vertex
r51	x.1b	off 0.005 grid NTMadd vertex
r52	x.1b	off 0.005 grid LVTNMadd vertex
r53	x.1b	off 0.005 grid HVTPMadd vertex
r54	x.1b	off 0.005 grid LI1Madd vertex
r55	x.1b	off 0.005 grid LICM1add vertex
r56	x.1b	off 0.005 grid PSDMadd vertex
r57	x.1b	off 0.005 grid NSDMadd vertex
r58	x.1b	off 0.005 grid FOMadd vertex
r59	x.1b	off 0.005 grid PMM2mk vertex
r60	x.1b	off 0.005 grid CU1Mmk vertex
r61	x.1b	off 0.005 grid RPMmk vertex
r62	x.1b	off 0.005 grid PBOmk vertex
r63	x.1b	off 0.005 grid PDMmk vertex
r64	x.1b	off 0.005 grid NSMmk vertex
r65	x.1b	off 0.005 grid MM5mk vertex
r66	x.1b	off 0.005 grid VIM4mk vertex
r67	x.1b	off 0.005 grid MM4mk vertex

continues on next page

Table 5.96 – continued from previous page

ID	Name	Description
r68	x.1b	off 0.005 grid VIM3mk vertex
r69	x.1b	off 0.005 grid MM3mk vertex
r70	x.1b	off 0.005 grid VIM2mk vertex
r71	x.1b	off 0.005 grid CTM1mk vertex
r72	x.1b	off 0.005 grid LI1Mmk vertex
r73	x.1b	off 0.005 grid LICM1mk vertex
r74	x.1b	off 0.005 grid PSDMmk vertex
r75	x.1b	off 0.005 grid NSDMmk vertex
r76	x.1b	off 0.005 grid LDNTMmk vertex
r77	x.1b	off 0.005 grid NPCMmk vertex
r78	x.1b	off 0.005 grid HVNTMmk vertex
r79	x.1b	off 0.005 grid NTMmk vertex
r80	x.1b	off 0.005 grid LVOMmk vertex
r81	x.1b	off 0.005 grid ONOMmk vertex
r82	x.1b	off 0.005 grid TUNMmk vertex
r83	x.1b	off 0.005 grid HVTRMmk vertex
r84	x.1b	off 0.005 grid HVTPMmk vertex
r85	x.1b	off 0.005 grid LVTNMmk vertex
r86	x.1b	off 0.005 grid NWMmk vertex
r87	x.1b	off 0.005 grid DNMmk vertex
r88	x.1b	off 0.005 grid FOMmk vertex
r89	x.1b	off 0.005 grid cfom vertex
r90	x.1b	off 0.005 grid clvtnm vertex
r91	x.1b	off 0.005 grid chvtpm vertex
r92	x.1b	off 0.005 grid conom vertex
r93	x.1b	off 0.005 grid clvom vertex
r94	x.1b	off 0.005 grid cntm vertex
r95	x.1b	off 0.005 grid chvntm vertex
r96	x.1b	off 0.005 grid cnpc vertex
r97	x.1b	off 0.005 grid cnsdm vertex
r98	x.1b	off 0.005 grid cpsdm vertex
r99	x.1b	off 0.005 grid cli1m vertex
r100	x.1b	off 0.005 grid cviam3 vertex
r101	x.1b	off 0.005 grid cviam4 vertex
r102	x.1a	off 0.001 grid P1Mmk vertex
r103	x.1a	off 0.001 grid P1Madd vertex
r104	x.1a	off 0.001 grid P1Mdrop vertex
r105	x.1a	off 0.001 grid VIMmk vertex
r106	x.1a	off 0.001 grid MM1mk vertex
r107	x.1a	off 0.001 grid MM2mk vertex
r108	x.1a	off 0.001 grid pmm vertex
r109	x.1a	off 0.001 grid rdl vertex
r110	x.1a	off 0.001 grid pmm2 vertex
r111	x.1a	off 0.001 grid ubm vertex
r112	x.1a	off 0.001 grid bump vertex
r113	x.2	non-manhattan diffNOtSealUHVI edge
r114	x.2	non-manhattan tapNotSealUHVI edge
r115	x.2	non-manhattan poly_noESD_noAnch edge
r116	x.2	non-manhattan li1Peri_noSEAL_noAnch edge
r117	x.2	non-manhattan licon_nonSEAL edge

continues on next page

Table 5.96 – continued from previous page

ID	Name	Description
r118	x.2	non-manhattan mcon_nonSEAL edge
r119	x.2	non-manhattan via_nonSEAL edge
r120	x.2	non-manhattan via2_nonSEAL edge
r121	x.2	non-manhattan via3_nonSEAL edge
r122	x.2	non-manhattan via4_nonSEAL edge
r123	x.2a	difftap enclosed in areaid.analog must be rectangular
r124	x.3a	non-octagonal nwell edge
r125	x.3a	non-octagonal diff edge
r126	x.3a	non-octagonal dnwell edge
r127	x.3a	non-octagonal lvtn edge
r128	x.3a	non-octagonal hvtp edge
r129	x.3a	non-octagonal hvi edge
r130	x.3a	non-octagonal tunm edge
r131	x.3a	non-octagonal npc edge
r132	x.3a	non-octagonal nsdm edge
r133	x.3a	non-octagonal psdm edge
r134	x.3a	non-octagonal met1 edge
r135	x.3a	non-octagonal met2 edge
r136	x.3a	non-octagonal vhvi edge
r137	x.3a	non-octagonal met3 edge
r138	x.3a	non-octagonal met4 edge
r139	x.3a	non-octagonal met5 edge
r140	x.3a	non-octagonal nsm edge
r141	x.3a	non-octagonal pad edge
r142	x.3a	non-octagonal ldntm edge
r143	x.3a	non-octagonal hvntm edge
r144	x.3a	non-octagonal pnp edge
r145	x.3a	non-octagonal capacitor edge
r146	x.3a	non-octagonal ncm edge
r147	x.3a	non-octagonal inductor edge
r148	x.3a	non-octagonal rpm edge
r149	x.3a	non-octagonal hvtr edge
r150	x.3a	non-octagonal metop1 edge
r151	x.3a	non-octagonal metop2 edge
r152	x.3a	non-octagonal metop3 edge
r153	x.3a	non-octagonal metop4 edge
r154	x.3a	non-octagonal metop5 edge
r155	x.3a	non-octagonal metop6 edge
r156	x.3a	non-octagonal metop7 edge
r157	x.3a	non-octagonal metop8 edge
r158	x.3a	non-octagonal NTMdrop edge
r159	x.3a	non-octagonal LVTNMdrop edge
r160	x.3a	non-octagonal HVTPMdrop edge
r161	x.3a	non-octagonal LI1Mdrop edge
r162	x.3a	non-octagonal LICM1drop edge
r163	x.3a	non-octagonal PSDMdrop edge
r164	x.3a	non-octagonal NSDMdrop edge
r165	x.3a	non-octagonal P1Mdrop edge
r166	x.3a	non-octagonal FOMdrop edge
r167	x.3a	non-octagonal NTMadd edge

Table 5.96 – continued from previous page

ID	Name	Description
r168	x.3a	non-octagonal LVTNMadd edge
r169	x.3a	non-octagonal HVTPMadd edge
r170	x.3a	non-octagonal LI1Madd edge
r171	x.3a	non-octagonal LICM1add edge
r172	x.3a	non-octagonal PSDMadd edge
r173	x.3a	non-octagonal NSDMadd edge
r174	x.3a	non-octagonal P1Madd edge
r175	x.3a	non-octagonal FOMadd edge
r176	x.3a	non-octagonal cfom edge
r177	x.3a	non-octagonal clvtnm edge
r178	x.3a	non-octagonal chvtpm edge
r179	x.3a	non-octagonal conom edge
r180	x.3a	non-octagonal clvom edge
r181	x.3a	non-octagonal cntm edge
r182	x.3a	non-octagonal chvntm edge
r183	x.3a	non-octagonal cnpc edge
r184	x.3a	non-octagonal cnsdm edge
r185	x.3a	non-octagonal cpsdm edge
r186	x.3a	non-octagonal cli1m edge
r187	x.3a	non-octagonal cviam3 edge
r188	x.3a	non-octagonal cviam4 edge
r189	x.3a	non-octagonal PMM2mk edge
r190	x.3a	non-octagonal CU1Mmk edge
r191	x.3a	non-octagonal RPMmk edge
r192	x.3a	non-octagonal PBOmk edge
r193	x.3a	non-octagonal PDMmk edge
r194	x.3a	non-octagonal NSMmk edge
r195	x.3a	non-octagonal MM5mk edge
r196	x.3a	non-octagonal VIM4mk edge
r197	x.3a	non-octagonal MM4mk edge
r198	x.3a	non-octagonal VIM3mk edge
r199	x.3a	non-octagonal MM3mk edge
r200	x.3a	non-octagonal VIM2mk edge
r201	x.3a	non-octagonal MM2mk edge
r202	x.3a	non-octagonal VIMmk edge
r203	x.3a	non-octagonal MM1mk edge
r204	x.3a	non-octagonal CTM1mk edge
r205	x.3a	non-octagonal LI1Mmk edge
r206	x.3a	non-octagonal LICM1mk edge
r207	x.3a	non-octagonal PSDMmk edge
r208	x.3a	non-octagonal NSDMmk edge
r209	x.3a	non-octagonal LDNTMmk edge
r210	x.3a	non-octagonal NPCMmk edge
r211	x.3a	non-octagonal HVNTMmk edge
r212	x.3a	non-octagonal NTMmk edge
r213	x.3a	non-octagonal P1Mmk edge
r214	x.3a	non-octagonal LVOMmk edge
r215	x.3a	non-octagonal ONOMmk edge
r216	x.3a	non-octagonal TUNMmk edge
r217	x.3a	non-octagonal HVTRMmk edge

Table 5.96 – continued from previous page

ID	Name	Description
r218	x.3a	non-octagonal HVTPMmk edge
r219	x.3a	non-octagonal LVTNMmk edge
r220	x.3a	non-octagonal NWMmk edge
r221	x.3a	non-octagonal DNMmk edge
r222	x.3a	non-octagonal FOMmk edge
r223	x.3a	non-octagonal tap_SEAL edge
r224	x.3a	non-octagonal tap_ENID edge
r225	x.3a	non-octagonal poly_ESD edge
r226	x.3a	non-octagonal "li1" in core edge
r227	x.3a	non-octagonal li1_SEAL edge
r228	x.3a	non-octagonal licon_SEAL edge
r229	x.3a	non-octagonal mcon_SEAL edge
r230	x.3a	non-octagonal via_SEAL edge
r231	x.3a	non-octagonal via2_SEAL edge
r232	x.3a	non-octagonal via3_SEAL edge
r233	x.5	met5Pin must be enclosed by met5
r234	x.5	met4Pin must be enclosed by met4
r235	x.5	met3Pin must be enclosed by met3
r236	x.5	met2Pin must be enclosed by met2
r237	x.5	met1Pin must be enclosed by met1
r238	x.5	li1Pin must be enclosed by li1
r239	x.5	polyPin must be enclosed by poly
r240	x.5	diffPin must be enclosed by diff
r241	x.9	NTMdrop must be enclosed by COREID
r242	x.9	LVTNMdrop must be enclosed by COREID
r243	x.9	HVTPMdrop must be enclosed by COREID
r244	x.9	LI1Mdrop must be enclosed by COREID
r245	x.9	LICM1drop must be enclosed by COREID
r246	x.9	PSDMdrop must be enclosed by COREID
r247	x.9	NSDMdrop must be enclosed by COREID
r248	x.9	P1Mdrop must be enclosed by COREID
r249	x.9	NTMadd must be enclosed by COREID
r250	x.9	LVTNMadd must be enclosed by COREID
r251	x.9	HVTPMadd must be enclosed by COREID
r252	x.9	LI1Madd must be enclosed by COREID
r253	x.9	LICM1add must be enclosed by COREID
r254	x.9	PSDMadd must be enclosed by COREID
r255	x.9	NSDMadd must be enclosed by COREID
r256	x.9	P1Madd must be enclosed by COREID
r257	x.9	FOMadd must be enclosed by COREID
r258	x.9	FOM outside advSeal_6um must be enclosed by COREID
r259	x.10	diffres must not overlap licon1
r260	x.10	polyres must not overlap licon1
r261	x.12a	0.635 min. spacing of moduleCutAREA & q0nwellnotBuildSpace
r262	x.12b	0.635 min. enclosure of q0nwellnotBuildSpace by moduleCutAREA
r263	x.12a	0.135 min. spacing of moduleCutAREA & q0diffnotBuildSpace
r264	x.12b	0.135 min. enclosure of q0diffnotBuildSpace by moduleCutAREA
r265	x.12a	3.15 min. spacing of moduleCutAREA & q0dnwellnotBuildSpace
r266	x.12b	3.15 min. enclosure of q0dnwellnotBuildSpace by moduleCutAREA
r267	x.12a	0.135 min. spacing of moduleCutAREA & q0tapnotBuildSpace

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ID	Name	Description
r268	x.12b	0.135 min. enclosure of q0tapnotBuildSpace by moduleCutAREA
r269	x.12a	0.19 min. spacing of moduleCutAREA & q0lvtnnotBuildSpace
r270	x.12b	0.19 min. enclosure of q0lvtnnotBuildSpace by moduleCutAREA
r271	x.12a	0.19 min. spacing of moduleCutAREA & q0hvtpnotBuildSpace
r272	x.12b	0.19 min. enclosure of q0hvtpnotBuildSpace by moduleCutAREA
r273	x.12a	0.35 min. spacing of moduleCutAREA & q0hvinotBuildSpace
r274	x.12b	0.35 min. enclosure of q0hvinotBuildSpace by moduleCutAREA
r275	x.12a	0.25 min. spacing of moduleCutAREA & q0tunmnotBuildSpace
r276	x.12b	0.25 min. enclosure of q0tunmnotBuildSpace by moduleCutAREA
r277	x.12a	0.105 min. spacing of moduleCutAREA & q0polynotBuildSpace
r278	x.12b	0.105 min. enclosure of q0polynotBuildSpace by moduleCutAREA
r279	x.12a	0.135 min. spacing of moduleCutAREA & q0npcnotBuildSpace
r280	x.12b	0.135 min. enclosure of q0npcnotBuildSpace by moduleCutAREA
r281	x.12a	0.19 min. spacing of moduleCutAREA & q0nsdmnotBuildSpace
r282	x.12b	0.19 min. enclosure of q0nsdmnotBuildSpace by moduleCutAREA
r283	x.12a	0.19 min. spacing of moduleCutAREA & q0psdmnotBuildSpace
r284	x.12b	0.19 min. enclosure of q0psdmnotBuildSpace by moduleCutAREA
r285	x.12a	0.085 min. spacing of moduleCutAREA & q0licon1notBuildSpace
r286	x.12b	0.085 min. enclosure of q0licon1notBuildSpace by moduleCutAREA
r287	x.12a	0.085 min. spacing of moduleCutAREA & q0li1notBuildSpace
r288	x.12b	0.085 min. enclosure of q0li1notBuildSpace by moduleCutAREA
r289	x.12a	0.095 min. spacing of moduleCutAREA & q0mconnotBuildSpace
r290	x.12b	0.095 min. enclosure of q0mconnotBuildSpace by moduleCutAREA
r291	x.12a	0.07 min. spacing of moduleCutAREA & q0met1notBuildSpace
r292	x.12b	0.07 min. enclosure of q0met1notBuildSpace by moduleCutAREA
r293	x.12a	0.085 min. spacing of moduleCutAREA & q0vianotBuildSpace
r294	x.12b	0.085 min. enclosure of q0vianotBuildSpace by moduleCutAREA
r295	x.12a	0.07 min. spacing of moduleCutAREA & q0met2notBuildSpace
r296	x.12b	0.07 min. enclosure of q0met2notBuildSpace by moduleCutAREA
r297	x.12a	0.1 min. spacing of moduleCutAREA & q0via2notBuildSpace
r298	x.12b	0.1 min. enclosure of q0via2notBuildSpace by moduleCutAREA
r299	x.12a	0.15 min. spacing of moduleCutAREA & q0met3notBuildSpace
r300	x.12b	0.15 min. enclosure of q0met3notBuildSpace by moduleCutAREA
r301	x.12a	0.1 min. spacing of moduleCutAREA & q0via3notBuildSpace
r302	x.12b	0.1 min. enclosure of q0via3notBuildSpace by moduleCutAREA
r303	x.12a	0.15 min. spacing of moduleCutAREA & q0met4notBuildSpace
r304	x.12b	0.15 min. enclosure of q0met4notBuildSpace by moduleCutAREA
r305	x.12a	0.4 min. spacing of moduleCutAREA & q0via4notBuildSpace
r306	x.12b	0.4 min. enclosure of q0via4notBuildSpace by moduleCutAREA
r307	x.12a	0.8 min. spacing of moduleCutAREA & q0met5notBuildSpace
r308	x.12b	0.8 min. enclosure of q0met5notBuildSpace by moduleCutAREA
r309	x.12a	2 min. spacing of moduleCutAREA & q0nsmnotBuildSpace
r310	x.12b	2 min. enclosure of q0nsmnotBuildSpace by moduleCutAREA
r311	x.12a	0.635 min. spacing of moduleCutAREA & q0padnotBuildSpace
r312	x.12b	0.635 min. enclosure of q0padnotBuildSpace by moduleCutAREA
r313	x.12a	0.35 min. spacing of moduleCutAREA & q0ldntmnotBuildSpace
r314	x.12b	0.35 min. enclosure of q0ldntmnotBuildSpace by moduleCutAREA
r315	x.12a	0.19 min. spacing of moduleCutAREA & q0hvntmnotBuildSpace
r316	x.12b	0.19 min. enclosure of q0hvntmnotBuildSpace by moduleCutAREA
r317	x.12a	0.19 min. spacing of moduleCutAREA & q0ncmnotBuildSpace

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ID	Name	Description
r318	x.12b	0.19 min. enclosure of q0ncmnotBuildSpace by moduleCutAREA
r319	x.12a	5 min. spacing of moduleCutAREA & q0rdlnotBuildSpace
r320	x.12b	5 min. enclosure of q0rdlnotBuildSpace by moduleCutAREA
r321	x.12a	0.19 min. spacing of moduleCutAREA & q0hvtrnotBuildSpace
r322	x.12b	0.19 min. enclosure of q0hvtrnotBuildSpace by moduleCutAREA
r323	x.12d	0.14 min. spacing of moduleCutAREA & q1met1notBuildSpace
r324	x.12e	0.14 min. enclosure of q1met1notBuildSpace by moduleCutAREA
r325	x.12d	0.14 min. spacing of moduleCutAREA & q1met2notBuildSpace
r326	x.18b	0.42 min. enclosure of capm by moduleCutAREA
r327	x.18a	0.42 min. spacing of moduleCutAREA & cap2m
r328	x.18b	0.42 min. enclosure of cap2m by moduleCutAREA
r329	x.12d	0.2 min. spacing of moduleCutAREA & q1met4notBuildSpace
r330	x.12e	0.2 min. enclosure of q1met4notBuildSpace by moduleCutAREA
r331	x.15a	X.15a: layer cfom allowed inside areaid:mt or inside areaid.sl or inside areaid.ft
r332	x.15a	X.15a: layer clvtnm allowed inside areaid:mt or inside areaid.sl or inside areaid.ft
r333	x.15a	X.15a: layer chvtpm allowed inside areaid:mt or inside areaid.sl or inside areaid.ft
r334	x.15a	X.15a: layer conom allowed inside areaid:mt or inside areaid.sl or inside areaid.ft
r335	x.15a	X.15a: layer clvom allowed inside areaid:mt or inside areaid.sl or inside areaid.ft
r336	x.15a	X.15a: layer cntm allowed inside areaid:mt or inside areaid.sl or inside areaid.ft
r337	x.15a	X.15a: layer chvntm allowed inside areaid:mt or inside areaid.sl or inside areaid.ft
r338	x.15a	X.15a: layer cnpc allowed inside areaid:mt or inside areaid.sl or inside areaid.ft
r339	x.15a	X.15a: layer cnsdm allowed inside areaid:mt or inside areaid.sl or inside areaid.ft
r340	x.15a	X.15a: layer cpsdm allowed inside areaid:mt or inside areaid.sl or inside areaid.ft
r341	x.15a	X.15a: layer cli1m allowed inside areaid:mt or inside areaid.sl or inside areaid.ft
r342	x.15a	X.15a: layer cviam3 allowed inside areaid:mt or inside areaid.sl or inside areaid.ft
r343	x.15a	X.15a: layer cviam4 allowed inside areaid:mt or inside areaid.sl or inside areaid.ft
r344	x.15a	X.15a: layer PMM2mk allowed inside areaid:mt or inside areaid.sl or inside areaid.ft
r345	x.15a	X.15a: layer CU1Mmk allowed inside areaid:mt or inside areaid.sl or inside areaid.ft
r346	x.15a	X.15a: layer RPMmk allowed inside areaid:mt or inside areaid.sl or inside areaid.ft
r347	x.15a	X.15a: layer PBOmk allowed inside areaid:mt or inside areaid.sl or inside areaid.ft
r348	x.15a	X.15a: layer PDMmk allowed inside areaid:mt or inside areaid.sl or inside areaid.ft
r349	x.15a	X.15a: layer NSMmk allowed inside areaid:mt or inside areaid.sl or inside areaid.ft
r350	x.15a	X.15a: layer MM5mk allowed inside areaid:mt or inside areaid.sl or inside areaid.ft
r351	x.15a	X.15a: layer VIM4mk allowed inside areaid:mt or inside areaid.sl or inside areaid.ft
r352	x.15a	X.15a: layer MM4mk allowed inside areaid:mt or inside areaid.sl or inside areaid.ft
r353	x.15a	X.15a: layer VIM3mk allowed inside areaid:mt or inside areaid.sl or inside areaid.ft
r354	x.15a	X.15a: layer MM3mk allowed inside areaid:mt or inside areaid.sl or inside areaid.ft
r355	x.15a	X.15a: layer VIM2mk allowed inside areaid:mt or inside areaid.sl or inside areaid.ft
r356	x.15a	X.15a: layer MM2mk allowed inside areaid:mt or inside areaid.sl or inside areaid.ft
r357	x.15a	X.15a: layer VIMmk allowed inside areaid:mt or inside areaid.sl or inside areaid.ft
r358	x.15a	X.15a: layer MM1mk allowed inside areaid:mt or inside areaid.sl or inside areaid.ft
r359	x.15a	X.15a: layer CTM1mk allowed inside areaid:mt or inside areaid.sl or inside areaid.ft
r360	x.15a	X.15a: layer LI1Mmk allowed inside areaid:mt or inside areaid.sl or inside areaid.ft
r361	x.15a	X.15a: layer LICM1mk allowed inside areaid:mt or inside areaid.sl or inside areaid.ft
r362	x.15a	X.15a: layer PSDMmk allowed inside areaid:mt or inside areaid.sl or inside areaid.ft
r363	x.15a	X.15a: layer NSDMmk allowed inside areaid:mt or inside areaid.sl or inside areaid.ft
r364	x.15a	X.15a: layer LDNTMmk allowed inside areaid:mt or inside areaid.sl or inside areaid.ft
r365	x.15a	X.15a: layer NPCMmk allowed inside areaid:mt or inside areaid.sl or inside areaid.ft
r366	x.15a	X.15a: layer HVNTMmk allowed inside areaid:mt or inside areaid.sl or inside areaid.ft
r367	x.15a	X.15a: layer NTMmk allowed inside areaid:mt or inside areaid.sl or inside areaid.ft

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ID	Name	Description
r368	x.15a	X.15a: layer P1Mmk allowed inside areaid:mt or inside areaid.sl or inside areaid.ft
r369	x.15a	X.15a: layer LVOMmk allowed inside areaid:mt or inside areaid.sl or inside areaid.ft
r370	x.15a	X.15a: layer ONOMmk allowed inside areaid:mt or inside areaid.sl or inside areaid.ft
r371	x.15a	X.15a: layer TUNMmk allowed inside areaid:mt or inside areaid.sl or inside areaid.ft
r372	x.15a	X.15a: layer HVTRMmk allowed inside areaid:mt or inside areaid.sl or inside areaid.ft
r373	x.15a	X.15a: layer HVTPMmk allowed inside areaid:mt or inside areaid.sl or inside areaid.ft
r374	x.15a	X.15a: layer LVTNMmk allowed inside areaid:mt or inside areaid.sl or inside areaid.ft
r375	x.15a	X.15a: layer NWMmk allowed inside areaid:mt or inside areaid.sl or inside areaid.ft
r376	x.15a	X.15a: layer DNMmk allowed inside areaid:mt or inside areaid.sl or inside areaid.ft
r377	x.15a	X.15a: layer FOMmk allowed inside areaid:mt or inside areaid.sl or inside areaid.ft
r378	x.16	extentDie must not overlap moduleCutAREA
r379	x.19	SEAL ring is not at origin (0,0)
r380	x.21	prune must overlap areaidMTorSC
r381	x.23b	diff must not straddle SEALID
r382	x.23c	tap must not overlap SEALID
r383	x.23c	poly must not overlap SEALID
r384	x.23c	li1 must not overlap SEALID
r385	x.23c	met1 must not overlap SEALID
r386	x.23c	met2 must not overlap SEALID
r387	x.23c	met3 must not overlap SEALID
r388	x.23c	met4 must not overlap SEALID
r389	x.23c	met5 must not overlap SEALID
r390	x.26	SEALID_6um must overlap diff
r391	x.25	pnp layer must be within specified fixed layout cells sky130rf_pnp/sky130rf_pnp5x
r392	x.28	6 min. width of SEALID
r393	dnwell.2	3 min. width of dnwell
r394	dnwell.3	6.3 min. spacing/notch of dnwellNotPhotoNotUHVI
r395	dnwell.4	dnwell must not overlap pnp
r396	ulvt.3	LOWVTID must not straddle uhvi
r397	dnwell.7	dnwell cannot straddle localSub
r398	nwell.1	0.84 min. width of nwell
r399	nwell.2a	1.27 min. spacing/notch of nwell
r400	nwell.4	nwell_nonUHVI must overlap metal contacted tap to nwell
r401	nwell.5	0.4 min. enclosure of dnwellNotTechCDLOWVTID by filledNwell
r402	nwell.5	dnwellNotTechCDLOWVTID must be enclosed by filledNwell
r403	nwell.6	1.03 min enclosure of nwellHole by dnwell
r404	nwell.7	4.5 min spacing between nwell and dnwell on separate nets
r405	hvtp.1	0.38 min. width of hvtp
r406	hvtp.2	0.38 min. spacing/notch of hvtp
r407	hvtp.3	0.18 min. enclosure of PFET_PERI by hvtp
r408	hvtp.4	0.18 min. spacing of PFET_PERI & hvtp
r409	hvtp.5	0.265 min. area of hvtp
r410	hvtp.6	0.265 min. area of hvtpHoles
r411	hvtp.c1	Min/Max enclosure of nwell by hvtp
r412	lvtn.1a	0.38 min. width of lvtn
r413	lvtn.2	0.38 min. spacing/notch of lvtn
r414	lvtn.3a	0.18 min. spacing of Gate in Periphery outside UHVI layer & "lvtn" in periphery
r415	lvtn.3b	0.19 min spacing of lvtn(peri) to pfet along S/D direction
r416	lvtn.4b	0.18 min. enclosure of Gate in Periphery outside UHVI layer by "lvtn" in periphery
r417	lvtn.9	0.38 min. spacing of lvtn & hvtp

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ID	Name	Description
r418	lvtn.9	lvtn must not overlap hvtp
r419	lvtn.10	0.38 min enclosure of lvtn by (nwell not overlapping Varactor Channel)
r420	lvtn.12	0.38 min. spacing of lvtn & coreNwell
r421	lvtn.13	0.265 min. area of lvtn
r422	lvtn.14	0.265 min. area of lvtnHoles
r423	hvtr.1	0.38 min. width of hvtr
r424	hvtr.2	0.38 min. spacing of hvtr & hvtp
r425	hvtr.2	hvtr must not overlap hvtp
r426	hvtr.3	0.18 min. enclosure of PFET by hvtr
r427	difftap.1	0.15 min. width of diff across areaid:ce
r428	difftap.1	0.15 min. width of diff in PERI
r429	diff-tap.c1	0.14 min. width of diff in COREID
r430	difftap.1	0.15 min. width of tap across areaid:ce
r431	difftap.1	0.15 min. width of tap in PERI
r432	diff-tap.c1	0.14 min. width of tap in COREID
r433	difftap.2	0.42 min. width of GATE_PERI_noSC
r434	diff-tap.2b	0.36 min. width of GATE_PERI_SC
r435	difftap.3	0.27 min. spacing/notch of diff or tap
r436	difftap.4	0.29 min. width of tap butting diff
r437	difftap.5	0.4 min. width of "tap" in periphery butting & between diff
r438	difftap.6	diff and tap are not allowed to extend beyond their abutting edge
r439	difftap.7	0.13 spacing of diff/tap butting edge to non-coincident diff/tap edge
r440	difftap.8	0.18 min. enclosure of PDIFF_PERI_nonESDuhvi by nwell
r441	difftap.9	0.34 min. spacing of NDIFF_PERI_nonESDuhvi & nwell_noesd
r442	diff-tap.10	0.18 min. enclosure of NTAP_nonESD_nonuhvi by nwell
r443	diff-tap.11	0.13 min. spacing of PTAP_nonUHVI & nwell
r444	diff-tap.c1	0.14 min. width of "gate" in core
r445	diff-tap.c5	0.38 min. width of "tap" in core butting & between diff
r446	diff-tap.c8	0.15 min. enclosure of "pdiff" in core by nwell
r447	diff-tap.c10	0.15 min. enclosure of "ntap" in core by nwell
r448	diff-tap.c12	0.18 min. enclosure of adj. sides of "pdiff" in core by nwell
r449	diff-tap.c13	0.32 min. spacing of "ndiff" in core & nwell
r450	diff-tap.c14	0.34 min. enclosure of adj. sides of "ndiff" in core by chipNotNwell
r451	tunm.1	0.41 min. width of tunm
r452	tunm.2	0.5 min. spacing/notch of tunm
r453	tunm.3	0.095 min. extension of tunm beyond gate
r454	tunm.4	0.095 min. spacing of GATE_outsidetunm & tunm
r455	tunm.5	gate must not straddle tunm

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ID	Name	Description
r456	tunm.6a	tunm outside deep nwell is not allowed
r457	tunm.7	0.672 min. area of tunm
r458	tunm.8	tunm must be enclosed by COREID
r459	nsd.1	0.38 min. width of nsdm across areaid:ce
r460	nsd.1	0.38 min. width of nsdm in PERI
r461	nsd.c1b	0.29 min. width of nsdm in COREID
r462	nsd.2	0.38 min. spacing/notch of "nsdm" in periphery
r463	nsd.2	0.38 min. spacing of nsdm across COREID boundary
r464	nsd.5a	0.125 min. enclosure of n+ diff by nsdm
r465	nsd.5b	0.125 min. enclosure of n+ tap in peri by nsdm
r466	nsd.7	0.13 min. spacing of nsdm & opposite implant diffTap
r467	nsd.8	nsdm must not overlap pdiff/ptap (source of extendedDrain fet exempted)
r468	nsd.9	ndiff/ntap (source of extendedDrain fet and gated_npn exempted) must be enclosed by nsdmZENERID
r469	nsd.10a	0.265 min. area of nsdm
r470	nsd.11	0.265 min. area of nsdmHole
r471	nsd.c1a	0.38 min. width of nsdm (opposite parallel)
r472	nsd.c2a	0.38 min. spacing/notch of "nsdm" in core
r473	nsd.c2b	0.29 min. spacing/notch of "nsdm" in core
r474	nsd.c5a	0.13 min. enclosure of n+ tap in core by nsdm
r475	psd.1	0.38 min. width of psdm across areaid:ce
r476	psd.1	0.38 min. width of psdm in PERI
r477	psd.c1b	0.29 min. width of psdm in COREID
r478	psd.2	0.38 min. spacing/notch of "psdm" in periphery
r479	psd.2	0.38 min. spacing of psdm across COREID boundary
r480	psd.5a	0.125 min. enclosure of p+ diff by psdm
r481	psd.5b	0.125 min. enclosure of p+ tap in peri by psdm
r482	psd.7	0.13 min. spacing of psdm & opposite implant diffTap
r483	psd.8	psdm must not overlap ndiff/ntap (source of extendedDrain fet exempted)
r484	psd.9	pdiff/ptap (source of extendedDrain fet exempted) must be enclosed by psdmZENERID
r485	psd.10b	0.255 min. area of psdm
r486	psd.11	0.265 min. area of psdmHole
r487	psd.c1a	0.38 min. width of psdm (opposite parallel)
r488	psd.c2a	0.38 min. spacing/notch of "psdm" in core
r489	psd.c2b	0.29 min. spacing/notch of "psdm" in core
r490	psd.c5b	0.12 min. enclosure of p+ tap in core by psdm
r491	hvi.1	0.6 min. width of hvi_peri
r492	hvi.2a	0.7 min. spacing/notch of hvi_peri
r493	hvi.4	hvi must not overlap tunm
r494	hvi.5	0.7 min. spacing between non-butting hvi and nwell
r495	nwell.8	2 min. spacing of HV_nwell & nwell
r496	hv.nwell.1	2.5 min. spacing of nwell with text (shv_nwell) & nwell
r497	nwell.9	HVnwell must be enclosed by hvi
r498	nwell.10	LVnwell should not be on the same net as HVnwell
r499	diff-tap.14	0.29 min. width of Hdiff in periphery not Hv Pdiff Res
r500	diff-tap.14a	0.15 min. width of Hv Pdiff Res in periphery
r501	diff-tap.15a	0.3 min. spacing/notch of Hdiff in periphery

Table 5.96 – continued from previous page

ID	Name	Description
r502	diff-tap.15b	0.37 min. spacing of n+ diff inside hvi in periphery & ptapHV_PERI_noAbut
r503	diff-tap.16	0.7 min. width of tapHV butting diffHV_noUHVI
r504	diff-tap.16	0.7 min. width of tapHV_noUHVI butting & between Hdiff
r505	diff-tap.17	0.33 min. enclosure of p+ Hdiff (no ESD)(no UHVI) by HV_nwell
r506	diff-tap.18	0.43 min. spacing of ndiff_nonESDuhvi & HV_nwell
r507	diff-tap.19	0.33 min. enclosure of n+ Htap (no ESD)(no UHVI) by HV_nwell
r508	diff-tap.20	0.43 min. spacing of PTAP_noPwellRes_noUHVI & HV_nwell
r509	diff-tap.21	"diffTap" in periphery must not straddle hvi
r510	diff-tap.22	0.18 min. enclosure of Hdiff/Htap in periphery without UHVI by hvi
r511	diff-tap.23	0.18 min. spacing of diffTapNoHv_PERI & hvi
r512	diff-tap.24	0.43 min. spacing of ndiffHV_nonESDuhvi & nwell
r513	diff-tap.c11	0.15 min. width of Hdiff in COREID
r514	poly.13	0.5 min. width of poly over diff inside hvi in periphery
r515	poly.14	gate must not straddle hvi
r516	poly.1a	0.15 min. width of poly
r517	poly.1b	poly.1b: 0.350 min. channel length of pfet overlapping lvtn
r518	poly.2	0.21 min. spacing/notch of "poly" in periphery
r519	poly.2	0.21 min. spacing of poly2noXmt across COREID boundary
r520	poly.c3	poly.c3: 0.175 min. spacing of poly (except for poly.c2)
r521	poly.c2	poly.c2: 0.160 min. spacing of poly for poly core gap
r522	poly.3	0.33 min. width of poly resistor
r523	poly.4	0.075 min. spacing of "poly" in periphery & diff
r524	poly.5	0.055 min. spacing of "poly" in periphery & tap
r525	poly.6	0.3 min. extension of diff edge butting tap beyond gate edge in periphery
r526	poly.7	0.25 min. extension of diff beyond gate edge in periphery
r527	poly.8	0.13 min. extension of poly beyond gate end in periphery
r528	poly.9	0.48 min. spacing of poly resistor & diffTap
r529	poly.9	poly resistor must not overlap diffTap
r530	poly.9	0.48 min. spacing of poly resistor & poly
r531	poly.10	poly must not overlap any inner corner of diff
r532	poly.11	No 90 degree bends of poly on diff
r533	poly.12	PolyNotLvNwellnoUHVI must not overlap "tap" in periphery
r534	poly.15	poly must not overlap diffres
r535	poly.c1	0.03 min. spacing of "poly" in core & diff
r536	poly.c1	0.03 min. spacing of "poly" in core & tap
r537	dnwell.6	rfNMOS must be enclosed by dnwell
r538	poly.x.1a	0.5 min. width of dummy_nhv
r539	poly.x.1a	0.15 min. width of dummy_nlowvt

Table 5.96 – continued from previous page

ID	Name	Description
r540	poly.x.1a	0.15 min. width of dummy_nshort
r541	poly.x.1a	0.15 min. width of dummy_pshort
r542	poly.x.1a	0.35 min. width of dummy_plowvt
r543	poly.x.1	This is an invalid nfet
r544	poly.x.1	This is an invalid pfet
r545	poly.x.1	This nhvnative is only allow in the FGR
r546	poly.x.1	This sky130rf_pmedlvt_W0p84_L0p15_2F device has an invalid W/L. Please see MRGA
r547	poly.x.1	This sky130rf_pshort_W3p0_L0p25_M4_b device has an invalid W/L. Please see MRGA
r548	poly.x.1	This sky130rf_pshort_W5p0_L0p15_2F device has an invalid W/L. Please see MRGA
r549	poly.x.1	This sky130rf_pshort_W1p65_L0p25_M4_b device has an invalid W/L. Please see MRGA
r551	poly.x.1	This sky130rf_pshort_W3p0_L0p15_M4_b device has an invalid W/L. Please see MRGA
r552	poly.x.1	This sky130rf_pshort_W5p0_L0p25_M4_b device has an invalid W/L. Please see MRGA
r553	poly.x.1	This sky130rf_pshort_W5p0_L0p25_M2_b device has an invalid W/L. Please see MRGA
r555	poly.x.1	This sky130rf_pshort_W0p84_L0p15_2F device has an invalid W/L. Please see MRGA
r556	poly.x.1	This sky130rf_pshort_W1p65_L0p25_M2_b device has an invalid W/L. Please see MRGA
r558	poly.x.1	This sky130rf_pshort_W3p0_L0p15_M2_b device has an invalid W/L. Please see MRGA
r559	poly.x.1	This sky130rf_pshort_W5p0_L0p15_M4_b device has an invalid W/L. Please see MRGA
r560	poly.x.1	This sky130rf_pshort_W5p0_L0p15_M2_b device has an invalid W/L. Please see MRGA
r561	poly.x.1	This sky130rf_pshort_W3p0_L0p15_2F device has an invalid W/L. Please see MRGA
r562	poly.x.1	This sky130rf_pshort_W5p0_L0p18_M4_b device has an invalid W/L. Please see MRGA
r563	poly.x.1	This sky130rf_pshort_W1p68_L0p15_4F device has an invalid W/L. Please see MRGA
r564	poly.x.1	This sky130rf_pshort_W3p0_L0p18_M4_b device has an invalid W/L. Please see MRGA
r565	poly.x.1	This sky130rf_pshort_W5p0_L0p18_M2_b device has an invalid W/L. Please see MRGA
r566	poly.x.1	This sky130rf_pshort_W3p0_L0p25_M2_b device has an invalid W/L. Please see MRGA
r567	poly.x.1	This sky130rf_pshort_W1p65_L0p15_M2_b device has an invalid W/L. Please see MRGA
r569	poly.x.1	This ppu device has an invalid W/L. Please see MRGA
r570	poly.x.1	This sky130rf_pshort_W1p68_L0p15_2F device has an invalid W/L. Please see MRGA
r571	poly.x.1	This sky130rf_pshort_W1p65_L0p18_M4_b device has an invalid W/L. Please see MRGA
r572	poly.x.1	This sky130rf_pmedlvt_W1p68_L0p15_4F device has an invalid W/L. Please see MRGA
r573	poly.x.1	This sky130rf_pshort_W1p65_L0p18_M2_b device has an invalid W/L. Please see MRGA
r574	poly.x.1	This sky130rf_pshort_W1p65_L0p15_M4_b device has an invalid W/L. Please see MRGA
r576	poly.x.1	This sky130rf_pshort_W3p0_L0p18_M2_b device has an invalid W/L. Please see MRGA
r577	poly.x.1	This sky130rf_pmedlvt_W1p68_L0p15_2F device has an invalid W/L. Please see MRGA
r578	poly.x.1	This sky130rf_nlowvt_W0p42_L0p15_2F device has an invalid W/L. Please see MRGA
r579	poly.x.1	This sky130rf_nlowvt_W0p84_L0p15_2F device has an invalid W/L. Please see MRGA
r580	poly.x.1	This sky130rf_nhv_W7p0_L0p5_M10_b device has an invalid W/L. Please see MRGA
r582	poly.x.1	This sky130rf_nshort_W5p0_L0p25_M4_b device has an invalid W/L. Please see MRGA
r583	poly.x.1	This npass device has an invalid W/L. Please see MRGA
r584	poly.x.1	This sky130rf_nlowvt_W1p65_L0p15_M2_b device has an invalid W/L. Please see MRGA
r585	poly.x.1	This sky130rf_nhv_W3p0_L0p5_M10_b device has an invalid W/L. Please see MRGA
r586	poly.x.1	This sonos_p device has an invalid W/L. Please see MRGA
r587	poly.x.1	This nhvnativeesd device has an invalid W/L. Please see MRGA
r588	poly.x.1	This npd device has an invalid W/L. Please see MRGA
r589	poly.x.1	This ntvnative device has an invalid W/L. Please see MRGA
r590	poly.x.1	This sky130rf_nhv_W5p0_L0p5_M4_b device has an invalid W/L. Please see MRGA
r591	poly.x.1	This sky130rf_nshort_W1p65_L0p18_M4_b device has an invalid W/L. Please see MRGA
r592	poly.x.1	This sky130rf_nlowvt_W3p0_L0p15_4F device has an invalid W/L. Please see MRGA
r593	poly.x.1	This fnpass device has an invalid W/L. Please see MRGA
r594	poly.x.1	This sky130rf_nlowvt_W1p65_L0p15_M4_b device has an invalid W/L. Please see MRGA
r595	poly.x.1	This sky130rf_nlowvt_W3p0_L0p18_M4_b device has an invalid W/L. Please see MRGA

Table 5.96 – continued from previous page

ID	Name	Description
r596	poly.x.1	This sky130rf_nlowvt_W3p0_L0p15_8F device has an invalid W/L. Please see MRGA
r597	poly.x.1	This sky130rf_nlowvt_W3p0_L0p15_M4_b device has an invalid W/L. Please see MRGA
r598	poly.x.1	This sky130rf_nlowvt_W3p0_L0p25_M4_b device has an invalid W/L. Please see MRGA
r599	poly.x.1	This sky130rf_nlowvt_W3p0_L0p15_M2_b device has an invalid W/L. Please see MRGA
r600	poly.x.1	This sky130rf_nlowvt_W5p0_L0p15_M2_b device has an invalid W/L. Please see MRGA
r601	poly.x.1	This sky130rf_nlowvt_W0p84_L0p15_4F device has an invalid W/L. Please see MRGA
r602	poly.x.1	This sky130rf_nshort_W3p0_L0p18_M4_b device has an invalid W/L. Please see MRGA
r603	poly.x.1	This sky130rf_nshort_W5p0_L0p18_M2_b device has an invalid W/L. Please see MRGA
r604	poly.x.1	This sky130rf_nshort_W5p0_L0p25_M2_b device has an invalid W/L. Please see MRGA
r606	poly.x.1	This sky130rf_nshort_W3p0_L0p25_M2_b device has an invalid W/L. Please see MRGA
r607	poly.x.1	This sonos_e device has an invalid W/L. Please see MRGA
r608	poly.x.1	This sky130rf_nshort_W5p0_L0p15_M4_b device has an invalid W/L. Please see MRGA
r609	poly.x.1	This sky130rf_nhv_W3p0_L0p5_M4_b device has an invalid W/L. Please see MRGA
r610	poly.x.1	This sky130rf_nlowvt_W3p0_L0p18_M2_b device has an invalid W/L. Please see MRGA
r611	poly.x.1	This sky130rf_nshort_W1p65_L0p25_M4_b device has an invalid W/L. Please see MRGA
r612	poly.x.1	This sky130rf_nshort_W3p0_L0p15_M2_b device has an invalid W/L. Please see MRGA
r614	poly.x.1	This sky130rf_nshort_W5p0_L0p15_M2_b device has an invalid W/L. Please see MRGA
r615	poly.x.1	This sky130rf_nhv_W5p0_L0p5_M2_b device has an invalid W/L. Please see MRGA
r616	poly.x.1	This sky130rf_nlowvt_W0p84_L0p15_8F device has an invalid W/L. Please see MRGA
r617	poly.x.1	This sky130rf_nshort_W1p65_L0p15_M4_b device has an invalid W/L. Please see MRGA
r618	poly.x.1	This sky130rf_nlowvt_W3p0_L0p25_M2_b device has an invalid W/L. Please see MRGA
r619	poly.x.1	This sky130rf_nlowvt_W5p0_L0p25_M4_b device has an invalid W/L. Please see MRGA
r620	poly.x.1	This nshortesd device has an invalid W/L. Please see MRGA
r621	poly.x.1	This sky130rf_nlowvt_W5p0_L0p25_M2_b device has an invalid W/L. Please see MRGA
r622	poly.x.1	This sky130rf_nshort_W3p0_L0p15_M4_b device has an invalid W/L. Please see MRGA
r624	poly.x.1	This sky130rf_nshort_W5p0_L0p18_M4_b device has an invalid W/L. Please see MRGA
r625	poly.x.1	This sky130rf_nlowvt_W1p65_L0p25_M2_b device has an invalid W/L. Please see MRGA
r626	poly.x.1	This sky130rf_nhv_W5p0_L0p5_M10_b device has an invalid W/L. Please see MRGA
r627	poly.x.1	This sky130rf_nshort_W3p0_L0p25_M4_b device has an invalid W/L. Please see MRGA
r628	poly.x.1	This sky130rf_nhv_W3p0_L0p5_M2_b device has an invalid W/L. Please see MRGA
r629	poly.x.1	This sky130rf_nlowvt_W1p65_L0p18_M2_b device has an invalid W/L. Please see MRGA
r630	poly.x.1	This nlvtpass device has an invalid W/L. Please see MRGA
r631	poly.x.1	This sky130rf_nshort_W1p65_L0p18_M2_b device has an invalid W/L. Please see MRGA
r632	poly.x.1	This sky130rf_nlowvt_W5p0_L0p15_M4_b device has an invalid W/L. Please see MRGA
r633	poly.x.1	This sky130rf_nlowvt_W1p65_L0p18_M4_b device has an invalid W/L. Please see MRGA
r634	poly.x.1	This sky130rf_nlowvt_W5p0_L0p18_M4_b device has an invalid W/L. Please see MRGA
r635	poly.x.1	This sky130rf_nlowvt_W3p0_L0p15_2F device has an invalid W/L. Please see MRGA
r636	poly.x.1	This sky130rf_nshort_W3p0_L0p18_M2_b device has an invalid W/L. Please see MRGA
r637	poly.x.1	This sky130rf_nlowvt_W5p0_L0p18_M2_b device has an invalid W/L. Please see MRGA
r638	poly.x.1	This sky130rf_nhv_W7p0_L0p5_M4_b device has an invalid W/L. Please see MRGA
r639	poly.x.1	This nhvesd device has an invalid W/L. Please see MRGA
r640	poly.x.1	This sky130rf_nshort_W1p65_L0p25_M2_b device has an invalid W/L. Please see MRGA
r641	poly.x.1	This sky130rf_nlowvt_W1p65_L0p25_M4_b device has an invalid W/L. Please see MRGA
r642	poly.x.1	This sky130rf_nshort_W1p65_L0p15_M2_b device has an invalid W/L. Please see MRGA
r643	poly.x.1	This pvhv device has an invalid W/L. Please see MRGA
r644	poly.x.1	This nvhv device has an invalid W/L. Please see MRGA
r645	diff.13	sky130rf_nlowvt_W0p42_L0p15_2F_cell should be rectangular
r646	diff.13	0.42 min. width of sky130rf_nlowvt_W0p42_L0p15_2F_cell
r647	diff.13	0.42 max. width of sky130rf_nlowvt_W0p42_L0p15_2F_cell
r648	diff.13	1.14 min. length of sky130rf_nlowvt_W0p42_L0p15_2F_cell

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ID	Name	Description
r649	diff.13	1.14 max. length of sky130rf_nlowvt_W0p42_L0p15_2F_cell
r650	diff.13	sky130rf_nlowvt_W0p84_L0p15_2F_cell should be rectangular
r651	diff.13	0.84 min. width of sky130rf_nlowvt_W0p84_L0p15_2F_cell
r652	diff.13	0.84 max. width of sky130rf_nlowvt_W0p84_L0p15_2F_cell
r653	diff.13	1.14 min. length of sky130rf_nlowvt_W0p84_L0p15_2F_cell
r654	diff.13	1.14 max. length of sky130rf_nlowvt_W0p84_L0p15_2F_cell
r655	diff.13	sky130rf_nlowvt_W0p84_L0p15_4F_cell should be rectangular
r656	diff.13	0.84 min. width of sky130rf_nlowvt_W0p84_L0p15_4F_cell
r657	diff.13	0.84 max. width of sky130rf_nlowvt_W0p84_L0p15_4F_cell
r658	diff.13	2 min. length of sky130rf_nlowvt_W0p84_L0p15_4F_cell
r659	diff.13	2 max. length of sky130rf_nlowvt_W0p84_L0p15_4F_cell
r660	diff.13	sky130rf_nlowvt_W0p84_L0p15_8F_cell should be rectangular
r661	diff.13	0.84 min. width of sky130rf_nlowvt_W0p84_L0p15_8F_cell
r662	diff.13	0.84 max. width of sky130rf_nlowvt_W0p84_L0p15_8F_cell
r663	diff.13	3.72 min. length of sky130rf_nlowvt_W0p84_L0p15_8F_cell
r664	diff.13	3.72 max. length of sky130rf_nlowvt_W0p84_L0p15_8F_cell
r665	diff.13	sky130rf_nlowvt_W3p0_L0p15_2F_cell should be rectangular
r666	diff.13	1.14 min. width of sky130rf_nlowvt_W3p0_L0p15_2F_cell
r667	diff.13	1.14 max. width of sky130rf_nlowvt_W3p0_L0p15_2F_cell
r668	diff.13	3 min. length of sky130rf_nlowvt_W3p0_L0p15_2F_cell
r669	diff.13	3 max. length of sky130rf_nlowvt_W3p0_L0p15_2F_cell
r670	diff.13	sky130rf_nlowvt_W3p0_L0p15_4F_cell should be rectangular
r671	diff.13	2 min. width of sky130rf_nlowvt_W3p0_L0p15_4F_cell
r672	diff.13	2 max. width of sky130rf_nlowvt_W3p0_L0p15_4F_cell
r673	diff.13	3 min. length of sky130rf_nlowvt_W3p0_L0p15_4F_cell
r674	diff.13	3 max. length of sky130rf_nlowvt_W3p0_L0p15_4F_cell
r675	diff.13	sky130rf_nlowvt_W3p0_L0p15_8F_cell should be rectangular
r676	diff.13	3 min. width of sky130rf_nlowvt_W3p0_L0p15_8F_cell
r677	diff.13	3 max. width of sky130rf_nlowvt_W3p0_L0p15_8F_cell
r678	diff.13	3.72 min. length of sky130rf_nlowvt_W3p0_L0p15_8F_cell
r679	diff.13	3.72 max. length of sky130rf_nlowvt_W3p0_L0p15_8F_cell
r680	diff.13	sky130rf_pshort_W0p84_L0p15_2F_cell should be rectangular
r681	diff.13	0.84 min. width of sky130rf_pshort_W0p84_L0p15_2F_cell
r682	diff.13	0.84 max. width of sky130rf_pshort_W0p84_L0p15_2F_cell
r683	diff.13	1.11 min. length of sky130rf_pshort_W0p84_L0p15_2F_cell
r684	diff.13	1.11 max. length of sky130rf_pshort_W0p84_L0p15_2F_cell
r685	diff.13	sky130rf_pshort_W1p68_L0p15_2F_cell should be rectangular
r686	diff.13	1.11 min. width of sky130rf_pshort_W1p68_L0p15_2F_cell
r687	diff.13	1.11 max. width of sky130rf_pshort_W1p68_L0p15_2F_cell
r688	diff.13	1.68 min. length of sky130rf_pshort_W1p68_L0p15_2F_cell
r689	diff.13	1.68 max. length of sky130rf_pshort_W1p68_L0p15_2F_cell
r690	diff.13	sky130rf_pshort_W1p68_L0p15_4F_cell should be rectangular
r691	diff.13	1.68 min. width of sky130rf_pshort_W1p68_L0p15_4F_cell
r692	diff.13	1.68 max. width of sky130rf_pshort_W1p68_L0p15_4F_cell
r693	diff.13	1.97 min. length of sky130rf_pshort_W1p68_L0p15_4F_cell
r694	diff.13	1.97 max. length of sky130rf_pshort_W1p68_L0p15_4F_cell
r695	diff.13	sky130rf_pshort_W3p0_L0p15_2F_cell should be rectangular
r696	diff.13	1.11 min. width of sky130rf_pshort_W3p0_L0p15_2F_cell
r697	diff.13	1.11 max. width of sky130rf_pshort_W3p0_L0p15_2F_cell
r698	diff.13	3 min. length of sky130rf_pshort_W3p0_L0p15_2F_cell

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ID	Name	Description
r699	diff.13	3 max. length of sky130rf_pshort_W3p0_L0p15_2F_cell
r700	diff.13	sky130rf_pshort_W5p0_L0p15_2F_cell should be rectangular
r701	diff.13	1.11 min. width of sky130rf_pshort_W5p0_L0p15_2F_cell
r702	diff.13	1.11 max. width of sky130rf_pshort_W5p0_L0p15_2F_cell
r703	diff.13	5 min. length of sky130rf_pshort_W5p0_L0p15_2F_cell
r704	diff.13	5 max. length of sky130rf_pshort_W5p0_L0p15_2F_cell
r705	poly.16	Poly of the RF FETs defined in Table H5 cannot overlap
r706	npc.1	0.27 min. width of npc
r707	npc.2	0.27 min. spacing/notch of npc
r708	npc.4	0.09 min. spacing of npc & gate
r709	npc.4	npc must not overlap gate
r710	npc.5	0.095 max enclosure of poly overlapping slotted_licon by npcm
r711	licon.2	0.17 min. spacing/notch of "licon1" in periphery
r712	licon.2	0.17 min. spacing of licon1 across COREID boundary
r713	licon.3	0.17 min. width of ring licon1
r714	licon.3	0.175 max. width of ring licon1
r715	licon.3	ring licon1 must be enclosed by SEALID
r716	licon.4	licon1 must overlap li1 and (poly or diff or tap)
r717	licon.5a	0.04 min. enclosure of "licon1" in periphery by diff
r718	licon.5b	0.06 min. spacing of tapLicon_PERI & diffTap butting edge
r719	licon.5c	0.06 min. enclosure of adj. sides of "licon1" in periphery by diff
r720	licon.6	"licon1" in periphery must not straddle tap
r721	licon.7	0.12 min. enclosure of adj. sides of "licon1" in periphery by noButtTap
r722	licon.8	0.05 min. enclosure of "poly_licon1" in periphery by poly
r723	licon.8a	0.08 min. enclosure of adj. sides of "poly_licon1" in periphery by poly
r724	licon.10	0.25 min. spacing of varLiconPer & varChannel
r725	licon.11	0.055 min. spacing of "licon1 on diffTap" in periphery & gateNoSC
r726	licon.11	"licon1 on diffTap" in periphery must not overlap gateNoSC
r727	li-con.11a	0.05 min. spacing of "licon1 on diffTap" in periphery & (gate and areaid.sc) except 0.15 phighvt
r728	li-con.11a	"licon1 on diffTap" in periphery must not overlap (gate and areaid.sc) except 0.15 phighvt
r729	li-con.11b	0.05 min. spacing of "licon1 on diffTap" in periphery & gateSCPhighvt
r730	li-con.11b	"licon1 on diffTap" in periphery must not overlap gateSCPhighvt
r731	li-con.11c	0.04 min. spacing of "licon1 on diffTap" in periphery & licon11cGate
r732	li-con.11c	"licon1 on diffTap" in periphery must not overlap licon11cGate
r733	li-con.11d	0.045 min. spacing of "licon1 on diffTap" in periphery & licon11dGate
r734	li-con.11d	"licon1 on diffTap" in periphery must not overlap licon11dGate
r735	licon.1	rectLCON1OutRpm should be rectangular
r736	licon.1	0.17 min. width of rectLCON1OutRpm
r737	licon.1	0.17 max. length of rectLCON1OutRpm
r738	li-con.1b/c	rectLCON1AndRpm should be rectangular

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ID	Name	Description
r739	li-con.1b/c	0.19 min. width of rectLCON1AndRpm
r740	li-con.1b/c	0.19 max. width of rectLCON1AndRpm
r741	li-con.1b/c	2 min. length of rectLCON1AndRpm
r742	li-con.1b/c	2 max. length of rectLCON1AndRpm
r743	licon.2b	0.35 min. spacing/notch of rectLCON1AndRpm
r744	licon.2c	min spacing between slotted licon in lateral dir is 0.510
r745	licon.2d	0.51 min. spacing of rectLCON1AndRpm & rectLCON1OutRpm
r746	licon.9	0.11 min. spacing of polyLicon1OutRpm & psdm
r747	licon.9	polyLicon1OutRpm must not overlap psdm
r748	licon.13	0.09 min. spacing of "licon1 on diffTap" in periphery & npc
r749	licon.13	"licon1 on diffTap" in periphery must not overlap npc
r750	licon.14	0.19 min. spacing of poly_licon1 & "diffTap" in periphery
r751	licon.15	0.1 min. enclosure of "poly_licon1" in periphery by npc
r752	licon.15	"poly_licon1" in periphery must be enclosed by npc
r753	npcon.c6	0.045 min. enclosure of "poly_licon1" in core by npc
r754	npcon.c6	"poly_licon1" in core must be enclosed by npc
r755	licon.16	source must enclose at least one licon in peri
r756	licon.16	tap must enclose at least one licon in peri
r757	licon.17	licon1 overlapping poly must not overlap diffTap
r758	licon.18	npc must enclose poly_licon
r759	licon.19	poly on HV varactor must not interact with licon
r760	licon.c1	0.13 min. spacing of poly_licon1 & "diffTap" in core
r761	licon.c3	0.165 min. spacing/notch of "licon1" in core
r762	licon.c4	"poly_licon1" in core must not overlap psdm
r763	li.1	0.17 min. width of liNoVppCaps across areaid:ce
r764	li.1	0.17 min. width of liNoVppCaps in PERI
r765	li.c1	0.14 min. width of liNoVppCaps in COREID
r766	li.1a	0.14 min. width of liVppCaps
r767	li.3	0.17 min. spacing/notch of li1_3_PERI
r768	li.3	0.17 min. spacing of li1 across COREID boundary
r769	li.3a	0.14 min. spacing/notch of li1_3a_PERI
r770	li.4	"licon1" in periphery must be enclosed by li1
r771	li.5	0.08 min. enclosure of adj. sides of "licon1" in periphery by li1
r772	li.6	0.0561 min. area of li1 across areaid:ce
r773	li.6	0.0561 min. area of li1
r774	li.7	0.29 min. width of li1AndResNoESD
r775	li.c1	0.14 min. width of "li1" in core
r776	li.c2	0.14 min. spacing/notch of "li1" in core
r777	ct.1	non-ring mcon should be rectangular
r778	ct.1	0.17 min. width of non-ring mcon
r779	ct.1	0.17 max. length of non-ring mcon
r780	ct.2	0.19 min. spacing/notch of mcon
r781	ct.3	0.17 min. width of ring-shaped mcon
r782	ct.3	0.175 max. width of ring-shaped mcon
r783	ct.3	ring-shaped mcon must be enclosed by SEALID
r784	ct.4	"mcon" in periphery must be enclosed by li1

Table 5.96 – continued from previous page

ID	Name	Description
r785	ct.c1	"mcon" in core must overlap li1
r786	ct.c2	0.19 min. spacing/notch of "mcon" in core
r787	m1.1	0.14 min. width of met1
r788	m1.2	0.14 min. spacing/notch of met1
r789	m1.3b	0.28 min. spacing between huge met1 and normal met1
r790	m1.3a	0.28 min. spacing/notch of huge met1+nearby met1
r791	m1.4	0.03 min. enclosure of mcon_PERI_4 by met1
r792	m1.4	mcon_PERI_4 must be enclosed by met1
r793	m1.4a	0.005 min. enclosure of mcon_PERI_4a by met1
r794	m1.4a	mcon_PERI_4a must be enclosed by met1
r795	m1.5	0.06 min. enclosure of adj. sides of "mcon" in periphery by met1
r796	m1.6	0.083 min. area of met1
r797	m1.7	0.14 min. area of met1Hole
r798	m1.7	0.14 min. area of met1HoleEmpty
r799	m1.c1	"mcon" in core must be enclosed by met1
r800	via.1a	via outside of moduleCut should be rectangular
r801	via.1a	0.15 min. width of via outside of moduleCut
r802	via.1a	0.15 max. length of via outside of moduleCut
r803	via.1b	via size inside module cut must be 0.150 or 0.230 or 0.280
r804	via.2	0.17 min. spacing/notch of via
r805	via.3	0.2 min. width of ring-shaped via
r806	via.3	0.205 max. width of ring-shaped via
r807	via.3	ring-shaped via must be enclosed by SEALID
r808	via.4a	0.055 min. enclosure of 0.15um via by met1
r809	via.4a	0.15um via must be enclosed by met1
r810	via.4b	0.03 min. enclosure of 0.23 via within modulecut by met1
r811	via.4b	0.23 via within modulecut must be enclosed by met1
r812	via.4c	0 min. enclosure of 0.28 via within modulecut by met1
r813	via.4c	0.28 via within modulecut must be enclosed by met1
r814	via.5a	0.085 min. enclosure of adj. sides of 0.15um via by met1
r815	via.5b	0.06 min. enclosure of adj. sides of 0.23 via within modulecut by met1
r816	via.5c	0 min. enclosure of adj. sides of 0.28 via within modulecut by met1
r817	m2.1	0.14 min. width of met2
r818	m2.2	0.14 min. spacing/notch of met2
r819	m2.3b	0.28 min. spacing between huge met2 and normal met2
r820	m2.3a	0.28 min. spacing/notch of huge met2+nearby met2
r821	m2.4	0.055 min. enclosure of "via" in periphery by met2
r822	m2.4	"via" in periphery must be enclosed by met2
r823	m2.5	0.085 min. enclosure of adj. sides of via by met2
r824	m2.6	0.0676 min. area of met2
r825	m2.7	0.14 min. area of met2Hole
r826	m2.7	0.14 min. area of met2HoleEmpty
r827	m2.c4	0.04 min. enclosure of "via" in core by met2
r828	m2.c4	"via" in core must be enclosed by met2
r829	varac.1	Min channel length of varactor channel is 0.180
r830	varac.2	Min channel width of varactor channel is 1.000
r831	varac.3	0.18 min. spacing of varChannel & hvtp
r832	varac.4	0.25 min. spacing of varChannel & liconOnTap
r833	varac.5	0.15 min. enclosure of polyonVarChannel by nwell
r834	varac.6	0.27 min. spacing of taponVarChannel & difftapNotVarChannel

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ID	Name	Description
r835	varac.7	nwell overlapping varacChannel must not overlap p+ diff
r836	viatop.1	viatop should be rectangular
r837	viatop.1	0.42 min. width of viatop
r838	viatop.1	0.42 max. length of viatop
r839	viatop.2	0.42 min. spacing/notch of viatop
r840	viatop.3	Only min square ViaTop's are allowed
r841	viatop.4	0.29 min. enclosure of viatop by met5
r842	viatop.4	viatop must be enclosed by met5
r843	viatop.5	ViaTop must not be placed over Pad
r844	viatop.6	10.00 min. spacing of viatop to pad
r845	viatop.7	viatop connected to gate must be connected to antenna diode
r846	photo.11	0.215 min/max enclosure of tap by nwell inside photoDiode
r847	via2.1d	via size inside module cut must be 0.200, 0.280, 1.200, OR 1.500
r848	via2.1a	rectVIA2noMT should be rectangular
r849	via2.1a	0.2 min. width of rectVIA2noMT
r850	via2.1a	0.2 max. length of rectVIA2noMT
r851	via2.2	0.2 min. spacing/notch of via2
r852	via2.3	0.2 min. width of ring-shaped via2
r853	via2.3	0.205 max. width of ring-shaped via2
r854	via2.3	ring-shaped via2 must be enclosed by SEALID
r855	via2.4	0.04 min. enclosure of via2 by met2
r856	via2.4	via2 must be enclosed by met2
r857	via2.4a	0.14 min. enclosure of rectVIA2Big by met2
r858	via2.4a	rectVIA2Big must be enclosed by met2
r859	via2.5	0.085 min. enclosure of adj. sides of via2 by met2
r860	m3.1	0.3 min. width of met3
r861	m3.2	0.3 min. spacing/notch of met3
r862	m3.4	0.065 min. enclosure of via2 by met3
r863	m3.4	via2 must be enclosed by met3
r864	m3.6	0.24 min. area of met3
r865	m3.3d	0.4 min. spacing between huge met3 and normal met3
r866	m3.3c	0.4 min. spacing/notch of huge met3+nearby met3
r867	via3.1	rectVIA3noMT should be rectangular
r868	via3.1	0.2 min. width of rectVIA3noMT
r869	via3.1	0.2 max. length of rectVIA3noMT
r870	via3.1a	via size inside module cut must be 0.200 OR 0.800
r871	via3.2	0.2 min. spacing/notch of via3
r872	via3.3	0.2 min. width of ring-shaped via3
r873	via3.3	0.205 max. width of ring-shaped via3
r874	via3.3	ring-shaped via3 must be enclosed by SEALID
r875	via3.4	0.06 min. enclosure of non-ring via3 by met3
r876	via3.4	non-ring via3 must be enclosed by met3
r877	via3.5	0.09 min. enclosure of adj. sides of via3 by met3
r878	m4.1	0.3 min. width of met4
r879	m4.2	0.3 min. spacing/notch of met4
r880	m4.3	0.065 min. enclosure of via3 by met4
r881	m4.3	via3 must be enclosed by met4
r882	m4.4a	0.24 min. area of met4
r883	m4.5b	0.4 min. spacing between huge met4 and normal met4
r884	m4.5a	0.4 min. spacing/notch of huge met4+nearby met4

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ID	Name	Description
r885	via4.1	non-ring via4 should be rectangular
r886	via4.1	0.8 min. width of non-ring via4
r887	via4.1	0.8 max. length of non-ring via4
r888	via4.2	0.8 min. spacing/notch of via4
r889	via4.3	0.8 min. width of ring-shaped via4
r890	via4.3	0.805 max. width of ring-shaped via4
r891	via4.3	ring-shaped via4 must be enclosed by SEALID
r892	via4.4	0.19 min. enclosure of non-ring via4 by met4
r893	via4.4	non-ring via4 must be enclosed by met4
r894	m5.1	1.6 min. width of met5
r895	m5.2	1.6 min. spacing/notch of met5
r896	m5.3	0.31 min. enclosure of via4 by met5
r897	m5.3	via4 must be enclosed by met5
r898	m5.4	4 min. area of met5
r899	pad.2	1.27 min. spacing/notch of pad
r900	pad.3	hugepad with area less than 30000.0 not allowed
r901	den-mos.1	1.055 min. width of gate of Drain Extended nFET
r902	den-mos.2	0.28 min. width of deNFetSource not overlapping poly
r903	den-mos.3	0.925 min. width of deNFetSource overlapping poly
r904	den-mos.4	0.17 min. width of drain of Drain Extended nFET
r905	den-mos.5	min/max extension between de_nFET_source over nwell 0.225
r906	den-mos.6	min/max spacing between de_nFET_source and de_nFET_drain 1.585
r907	den-mos.7	min channel width 5.000
r908	den-mos.8	90 degree angles are not permitted for nwell over poly
r909	den-mos.10	0.66 min. enclosure of drain of Drain Extended nFET by nwell
r910	den-mos.11	0.86 min. spacing of ptap & nwellOVRdeNFetDrain
r911	den-mos.12	2.4 min. spacing of nwellOVRdeNFetDrain
r912	den-mos.13	0.13 min. enclosure of source of Drain Extended nFET by nsdm
r913	den-mos.13	source of Drain Extended nFET must be enclosed by nsdm
r915	dep-mos.1	1.05 min. width of gate of Drain Extended pFET
r916	dep-mos.2	0.28 min. width of dePFetSourceNotpoly
r917	dep-mos.3	0.92 min. width of dePFetSource overlapping poly
r918	dep-mos.4	0.17 min. width of drain of Drain Extended pFET

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ID	Name	Description
r919	dep-mos.5	min/max extension between de_pFET_source beyond nwell 0.260
r920	dep-mos.6	min/max spacing between de_pFET_source and de_pFET_drain 1.190
r921	dep-mos.7	min channel width 5.000
r922	dep-mos.8	90 degree angles are not permitted for nwellhole over poly
r923	pwde.6	1.00 min. enclosure of pwde_uhvi by dnwell_uhvi
r924	pwbm.5	0.84 min. spacing of pwbm_holes
r925	dep-mos.12	0.13 min. enclosure of source of Drain Extended pFET by psdm
r926	dep-mos.12	source of Drain Extended pFET must be enclosed by psdm
r927	dep-mos.13	pvhv_depmos13 must be enclosed by moduleCutAREA
r928	uhvi.6	UHVI must enclose dnwell
r929	uhvi.2	poly must not straddle uhvi
r930	extd.3	deFetPoly must overlap polyGap
r931	uhvi.3	pwbmNotLOWVTID must be enclosed by uhvi
r932	pwres.2	PwresDnw should be rectangular
r933	pwres.2	2.65 min. width of PwresDnw
r934	pwres.2	2.65 max. width of PwresDnw
r935	pwres.2	26.5 min. length of PwresDnw
r936	pwres.2	265 max. length of PwresDnw
r937	pwres.5	pwres Tap to nwell spacing must be 0.220
r938	pwres.6	0.53 min. width of PwresTerm
r939	pwres.6	Exceeds allowed width of pwell res tap
r940	pwres.7a	Tap in pwell must enclose 12 licon1
r941	pwres.7b	Tap in pwell must enclose 12 mcon
r942	pwres.8a	poly must not overlap PwresDnw
r943	pwres.8b	diff must not overlap PwresDnw
r944	pwres.9	Nwell around pwell res must have strapped tap with metal
r945	pwres.11	Pwell res must abut nwell edges on opposite sides
r946	pwres.10	Pwell res must abut 2 pwres_terminal on opposite sides
r947	rf-diode.1	non-manhattan RFDIODEID edge
r948	rf-diode.2	areaid.re must be coincident with nwell for the rf nwell diode
r949	rf-diode.3	areaid.re must be coincident with inner nwell ring edge for rf pwell-deep nwell diode
r950	nsm.1	3 min. width of nsm
r951	nsm.2	4 min. spacing/notch of nsm
r952	nsm.3	1 min. spacing of diff_not_NSM3_exempt & nsm OR NSMmk
r953	nsm.3	diff_not_NSM3_exempt must not overlap nsm OR NSMmk
r954	nsm.3	1 min. spacing of tap_not_NSM3_exempt & nsm OR NSMmk
r955	nsm.3	tap_not_NSM3_exempt must not overlap nsm OR NSMmk
r956	nsm.3	1 min. spacing of fomDummyDRC_not_NSM3_exempt & nsm OR NSMmk
r957	nsm.3	fomDummyDRC_not_NSM3_exempt must not overlap nsm OR NSMmk
r958	nsm.3	1 min. spacing of FOMmk_not_NSM3_exempt & nsm OR NSMmk

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ID	Name	Description
r959	nsm.3	FOMmk_not_NSM3_exempt must not overlap nsm OR NSMmk
r960	nsm.3	1 min. spacing of poly_not_NSM3_exempt & nsm OR NSMmk
r961	nsm.3	poly_not_NSM3_exempt must not overlap nsm OR NSMmk
r962	nsm.3	1 min. spacing of P1Mmk_not_NSM3_exempt & nsm OR NSMmk
r963	nsm.3	P1Mmk_not_NSM3_exempt must not overlap nsm OR NSMmk
r964	nsm.3	1 min. spacing of li1_not_NSM3_exempt & nsm OR NSMmk
r965	nsm.3	li1_not_NSM3_exempt must not overlap nsm OR NSMmk
r966	nsm.3	1 min. spacing of LI1Mmk_not_NSM3_exempt & nsm OR NSMmk
r967	nsm.3	LI1Mmk_not_NSM3_exempt must not overlap nsm OR NSMmk
r968	nsm.3	1 min. spacing of met1_not_NSM3_exempt & nsm OR NSMmk
r969	nsm.3	met1_not_NSM3_exempt must not overlap nsm OR NSMmk
r970	nsm.3	1 min. spacing of MM1mk_not_NSM3_exempt & nsm OR NSMmk
r971	nsm.3	MM1mk_not_NSM3_exempt must not overlap nsm OR NSMmk
r972	nsm.3	1 min. spacing of met2_not_NSM3_exempt & nsm OR NSMmk
r973	nsm.3	met2_not_NSM3_exempt must not overlap nsm OR NSMmk
r974	nsm.3	1 min. spacing of MM2Mk_not_NSM3_exempt & nsm OR NSMmk
r975	nsm.3	MM2Mk_not_NSM3_exempt must not overlap nsm OR NSMmk
r976	nsm.3	1 min. spacing of met3_not_NSM3_exempt & nsm OR NSMmk
r977	nsm.3	met3_not_NSM3_exempt must not overlap nsm OR NSMmk
r978	nsm.3	1 min. spacing of MM3mk_not_NSM3_exempt & nsm OR NSMmk
r979	nsm.3	MM3mk_not_NSM3_exempt must not overlap nsm OR NSMmk
r980	nsm.3	1 min. spacing of met4_not_NSM3_exempt & nsm OR NSMmk
r981	nsm.3	met4_not_NSM3_exempt must not overlap nsm OR NSMmk
r982	nsm.3	1 min. spacing of MM4mk_not_NSM3_exempt & nsm OR NSMmk
r983	nsm.3	MM4mk_not_NSM3_exempt must not overlap nsm OR NSMmk
r984	nsm.3	1 min. spacing of met5_not_NSM3_exempt & nsm OR NSMmk
r985	nsm.3	met5_not_NSM3_exempt must not overlap nsm OR NSMmk
r986	nsm.3	1 min. spacing of MM5mk_not_NSM3_exempt & nsm OR NSMmk
r987	nsm.3	MM5mk_not_NSM3_exempt must not overlap nsm OR NSMmk
r988	nsm.3a	3 min. enclosure of diff_not_NSM3a_exempt by frameBndr
r989	nsm.3a	3 min. enclosure of tap_not_NSM3a_exempt by frameBndr
r990	nsm.3a	3 min. enclosure of fomDummyDRC_not_NSM3a_exempt by frameBndr
r991	nsm.3a	3 min. enclosure of FOMmk_not_NSM3a_exempt by frameBndr
r992	nsm.3a	3 min. enclosure of poly_not_NSM3a_exempt by frameBndr
r993	nsm.3a	3 min. enclosure of P1Mmk_not_NSM3a_exempt by frameBndr
r994	nsm.3a	3 min. enclosure of li1_not_NSM3a_exempt by frameBndr
r995	nsm.3a	3 min. enclosure of LI1Mmk_not_NSM3a_exempt by frameBndr
r996	nsm.3a	3 min. enclosure of met1_not_NSM3a_exempt by frameBndr
r997	nsm.3a	3 min. enclosure of MM1mk_not_NSM3a_exempt by frameBndr
r998	nsm.3a	3 min. enclosure of met2_not_NSM3a_exempt by frameBndr
r999	nsm.3a	3 min. enclosure of MM2Mk_not_NSM3a_exempt by frameBndr
r1000	nsm.3a	3 min. enclosure of met3_not_NSM3a_exempt by frameBndr
r1001	nsm.3a	3 min. enclosure of MM3mk_not_NSM3a_exempt by frameBndr
r1002	nsm.3a	3 min. enclosure of met4_not_NSM3a_exempt by frameBndr
r1003	nsm.3a	3 min. enclosure of MM4mk_not_NSM3a_exempt by frameBndr
r1004	nsm.3a	3 min. enclosure of met5_not_NSM3a_exempt by frameBndr
r1005	nsm.3a	3 min. enclosure of MM5mk_not_NSM3a_exempt by frameBndr
r1006	nsm.3b	3 min. spacing of diff_not_NSM3b_exempt & dieCut
r1007	nsm.3b	3 min. spacing of tap_not_NSM3b_exempt & dieCut
r1008	nsm.3b	3 min. spacing of fomDummyDRC_not_NSM3b_exempt & dieCut

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ID	Name	Description
r1009	nsm.3b	3 min. spacing of FOMmk_not_NSM3b_exempt & dieCut
r1010	nsm.3b	3 min. spacing of poly_not_NSM3b_exempt & dieCut
r1011	nsm.3b	3 min. spacing of P1Mmk_not_NSM3b_exempt & dieCut
r1012	nsm.3b	3 min. spacing of li1_not_NSM3b_exempt & dieCut
r1013	nsm.3b	3 min. spacing of LI1Mmk_not_NSM3b_exempt & dieCut
r1014	nsm.3b	3 min. spacing of met1_not_NSM3b_exempt & dieCut
r1015	nsm.3b	3 min. spacing of MM1mk_not_NSM3b_exempt & dieCut
r1016	nsm.3b	3 min. spacing of met2_not_NSM3b_exempt & dieCut
r1017	nsm.3b	3 min. spacing of MM2Mk_not_NSM3b_exempt & dieCut
r1018	nsm.3b	3 min. spacing of met3_not_NSM3b_exempt & dieCut
r1019	nsm.3b	3 min. spacing of MM3mk_not_NSM3b_exempt & dieCut
r1020	nsm.3b	3 min. spacing of met4_not_NSM3b_exempt & dieCut
r1021	nsm.3b	3 min. spacing of MM4mk_not_NSM3b_exempt & dieCut
r1022	nsm.3b	3 min. spacing of met5_not_NSM3b_exempt & dieCut
r1023	nsm.3b	3 min. spacing of MM5mk_not_NSM3b_exempt & dieCut
r1024	ncm.x.3	ncm_CORE not tech_CD must not overlap "ndiff" in periphery
r1025	ncm.1	0.38 min. width of ncmPeri
r1026	ncm.2a	0.38 min. spacing/notch of ncmPeri
r1027	ncm.7	0.265 min. area of ncm
r1028	ncm.8	0.265 min. area of ncmHoles
r1029	ncm.c8	0.235 min. enclosure of PDIFF by ncm_CORE not tech_CD
r1030	ncm.c9	0.235 min. spacing of ncm_CORE not tech_CD & ndiff
r1031	ncm.c9	ncm_CORE not tech_CD must not overlap ndiff
r1032	ncm.c10	0.38 min. spacing of nwellOutCore & ncm_CORE not tech_CD
r1033	ld-ntm.c1	0.7 min. width of ldntmCore
r1034	ld-ntm.c2	0.7 min. spacing/notch of ldntmCore
r1035	ld-ntm.c3	enclosure of ndiff by ldntm must be more than 0.180
r1036	ld-ntm.c4	0.125 min. enclosure of nFet by ldntmCore
r1037	ld-ntm.c5	ldntm not allowed outside areaid.ce
r1038	ld-ntm.c6	0.18 min. spacing of ldntmCoreExempt & pdiff
r1039	urpm.1a	1.27 min. width of urpm
r1046	urpm.2	0.84 min. spacing/notch of urpm
r1047	urpm.3	0.2 min. enclosure of precResistor by rpm
r1048	rpm.3	precResistor must be enclosed by rpm
r1049	rpm.4	0.11 min. enclosure of precResistor by psdm
r1050	rpm.4	precResistor must be enclosed by psdm
r1051	rpm.5	0.095 min. enclosure of precResistor by npc
r1052	rpm.5	precResistor must be enclosed by npc
r1053	rpm.6	0.2 min. spacing of rpm & nsdm
r1054	rpm.6	rpm must not overlap nsdm
r1055	rpm.7	0.2 min. spacing of rpm & poly
r1056	rpm.8	poly must not straddle rpm
r1057	rpm.9	0.185 min. spacing of precResistor & hvntm
r1058	rpm.9	precResistor must not overlap hvntm

Table 5.96 – continued from previous page

ID	Name	Description
r1059	rpm.10	2 min. spacing of rpmNotXmt & pwbm
r1060	rpm.10	rpmNotXmt must not overlap pwbm
r1061	hvntm.x.1	hvntm must be drawn inside hvi
r1062	hvntm.1	0.7 min. width of hvntm_peri
r1063	hvntm.2	0.7 min. spacing/notch of hvntm_peri
r1064	hvntm.3	0.185 min. enclosure of ndiffInHviPeri by hvntm_peri
r1065	hvntm.4	0.185 min. spacing of hvntm_peri & ndiffOutsideHvi
r1066	hvntm.4	hvntm_peri must not overlap ndiffOutsideHvi
r1067	hvntm.5	0.185 min. spacing of hvntm_peri & PDIFF_notENID
r1068	hvntm.5	hvntm_peri must not overlap PDIFF_notENID
r1069	hvntm.6a	0.185 min. spacing of hvntm_peri & PTAPnoButtDiff
r1070	hvntm.6a	hvntm_peri must not overlap ptap
r1071	hvntm.6b	hvntm_peri must not overlap diffpTapButtEdge_sz
r1072	hvntm.7	0 min. enclosure of ESD_nwell_tap_hvi by hvntm_peri
r1073	hvntm.7	ESD_nwell_tap_hvi must be enclosed by hvntm_peri
r1074	hvntm.9	hvntm must not overlap COREID
r1075	hvntm.10	hvntm must overlap hvi
r1076	cfom.nikon	FOMmk in the nikon cross has the wrong polarity
r1077	cfom.nikon	FOMmk is missing from the nikon cross in the layout.
r1078	cdnm.nikon	DNMmk in the nikon cross has the wrong polarity
r1079	cdnm.nikon	DNMmk is missing from the nikon cross in the layout.
r1080	cnwm.nikon	NWMmk in the nikon cross has the wrong polarity
r1081	cnwm.nikon	NWMmk is missing from the nikon cross in the layout.
r1082	chvtpm.nikon	HVTPMmk in the nikon cross has the wrong polarity
r1083	chvtpm.nikon	HVTPMmk is missing from the nikon cross in the layout.
r1084	clvtnm.nikon	LVTNMmk in the nikon cross has the wrong polarity
r1085	clvtnm.nikon	LVTNMmk is missing from the nikon cross in the layout.
r1086	clvom.nikon	LVOMmk in the nikon cross has the wrong polarity
r1087	clvom.nikon	LVOMmk is missing from the nikon cross in the layout.
r1088	cp1m.nikon	P1Mmk in the nikon cross has the wrong polarity
r1089	cp1m.nikon	P1Mmk is missing from the nikon cross in the layout.
r1090	cntm.nikon	NTMmk in the nikon cross has the wrong polarity
r1091	cntm.nikon	NTMmk is missing from the nikon cross in the layout.
r1092	chvntm.nikon	HVNTMmk in the nikon cross has the wrong polarity
r1093	chvntm.nikon	HVNTMmk is missing from the nikon cross in the layout.
r1094	cld-ntm.nikon	LDNTMmk in the nikon cross has the wrong polarity
r1095	cld-ntm.nikon	LDNTMmk is missing from the nikon cross in the layout.
r1096	cnpc.nikon	NPCMmk in the nikon cross has the wrong polarity
r1097	cnpc.nikon	NPCMmk is missing from the nikon cross in the layout.
r1098	cnsdm.nikon	NSDMmk in the nikon cross has the wrong polarity
r1099	cnsdm.nikon	NSDMmk is missing from the nikon cross in the layout.
r1100	cpsdm.nikon	PSDMmk in the nikon cross has the wrong polarity
r1101	cpsdm.nikon	PSDMmk is missing from the nikon cross in the layout.
r1102	clicm1.nikon	LICM1mk in the nikon cross has the wrong polarity
r1103	clicm1.nikon	LICM1mk is missing from the nikon cross in the layout.
r1104	cli1m.nikon	LI1Mmk in the nikon cross has the wrong polarity
r1105	cli1m.nikon	LI1Mmk is missing from the nikon cross in the layout.
r1106	cctm1.nikon	CTM1mk in the nikon cross has the wrong polarity

Table 5.96 – continued from previous page

ID	Name	Description
r1107	cctm1.nik	CTM1mk is missing from the nikon cross in the layout.
r1108	cmm1.nik	MM1mk in the nikon cross has the wrong polarity
r1109	cmm1.nik	MM1mk is missing from the nikon cross in the layout.
r1110	cviam.nik	VIMmk in the nikon cross has the wrong polarity
r1111	cviam.nik	VIMmk is missing from the nikon cross in the layout.
r1112	cmm2.nik	MM2mk in the nikon cross has the wrong polarity
r1113	cmm2.nik	MM2mk is missing from the nikon cross in the layout.
r1114	cnsm.niko	NSMmk in the nikon cross has the wrong polarity
r1115	cnsm.niko	NSMmk is missing from the nikon cross in the layout.
r1116	cpdm.nikc	PDMmk in the nikon cross has the wrong polarity
r1117	cpdm.nikc	PDMmk is missing from the nikon cross in the layout.
r1118	cviam2.nil	VIM2mk in the nikon cross has the wrong polarity
r1119	cviam2.nil	VIM2mk is missing from the nikon cross in the layout.
r1120	cmm3.nik	MM3mk in the nikon cross has the wrong polarity
r1121	cmm3.nik	MM3mk is missing from the nikon cross in the layout.
r1122	cviam3.nil	VIM3mk in the nikon cross has the wrong polarity
r1123	cviam3.nil	VIM3mk is missing from the nikon cross in the layout.
r1124	cmm4.nik	MM4mk in the nikon cross has the wrong polarity
r1125	cmm4.nik	MM4mk is missing from the nikon cross in the layout.
r1126	cviam4.nil	VIM4mk in the nikon cross has the wrong polarity
r1127	cviam4.nil	VIM4mk is missing from the nikon cross in the layout.
r1128	cmm5.nik	MM5mk in the nikon cross has the wrong polarity
r1129	cmm5.nik	MM5mk is missing from the nikon cross in the layout.
r1130	crpm.niko	RPMmk in the nikon cross has the wrong polarity
r1131	crpm.niko	RPMmk is missing from the nikon cross in the layout.
r1132	areaid.1	Unapproved cells contain areaid.ce layer
r1133	vpp.5	1.5 min spacing of (li1, poly, or met1/2) overlapping cap.dg to other li1
r1134	vpp.5	1.5 min spacing of (li1, poly, or met1/2) overlapping cap.dg to other poly
r1135	vpp.5	1.5 min spacing of (li1, poly, or met1/2) overlapping cap.dg to other met1
r1136	vpp.5	1.5 min spacing of (li1, poly, or met1/2) overlapping cap.dg to other met2
r1137	vpp.5a	0.25 max PD ratio of met3.dg to capacitor.dg
r1138	vpp.5b	0.3 max PD ratio of met4.dg to capacitor.dg
r1139	vpp.5c	0.4 max PD ratio of met5.dg to capacitor.dg
r1140	vpp.10	capacitors are not allow to overlap
r1141	vpp.11	0.87 Minimum vpp_over_MOSCAP density over related gate
r1142	vpp.12a	capacitor in sky130rf2_xcmvpp8p6x7p9_m3_lim5shield must overlap only 9.0 met4 2.01x2.01 polygons
r1143	vpp.12b	capacitor in sky130rf2_xcmvpp11p5x11p7_m3_lim5shield must overlap only 16.0 met4 2.01x2.01 polygons
r1144	vpp.12c	capacitor in sky130rf2_xcmvpp4p4x4p6_m3_lim5shield must overlap only 4.0 met4 1.5x1.5 polygons
r1145	vpp.1	1.43 min. width of capacitor
r1146	vpp.1b	11.35 max. width of vpp_1b_err
r1147	vpp.1c	vppM3shieldA should be rectangular
r1148	vpp.1c	3.88 min. width of vppM3shieldA
r1149	vpp.1c	3.88 max. length of vppM3shieldA
r1150	vpp.3	vpp3NotXmt must not overlap poly
r1151	vpp.4	capacitor must not straddle nwell
r1152	vpp.4	capacitor must not straddle dnwell
r1153	vpp.8	1.5 min. enclosure of capacitor by nwell

Table 5.96 – continued from previous page

ID	Name	Description
r1154	vpp.9	1.5 min. spacing of capacitor & nwell
r1155	vhvi.vhv.5	diffusion not in drain-extended devices must not be connected to VHVSrcDrn
r1156	vhvi.1	0.02 min. width of vhvi
r1157	vhvi.2	vhvi must not overlap areaid.ce
r1158	vhvi.3	VHVGate must overlap hvi
r1159	vhvi.4	poly connected to same net as VHVsourcedrain must be tagged by vhvi
r1160	vhvi.5	vhvi must not straddle VHVSrcDrn
r1161	vhvi.6	vhvi overlapping VHVSrcDrn must not overlap poly
r1162	vhvi.7	vhvi must not straddle VHVPoly
r1163	vhvi.8	11.24 min. spacing of VHVnwell & VHVnwellNoConn
r1164	hv.diff.1a	Min space between hv_srcdrn and hv_srcdrn/diff for edges not butting tap is 0.3
r1165	hv.diff.1b	0.3 min. spacing of diffResButtHV & diff
r1166	hv.diff.1b	0.3 min. spacing of diffDiodeHV & diff
r1167	hv.diff.2	0.43 min. spacing of nwellConHVdiff & ndiff (not for source of drain extended device)
r1168	hv.diff.3a	0.55 min. spacing of HVnSrcDrn & nwell
r1169	hv.diff.3b	0.55 min. spacing of diffResButtHV & nwell
r1170	hv.diff.3b	0.55 min. spacing of diffDiodeHV & nwell
r1171	hv.poly.1	hv poly can be drawn over only one diff
r1172	hv.poly.1	hvPolyExmpt must not straddle nwell
r1173	hv.poly.1	hvpoly cannot cross nwell boundary (except nwell hole edge
r1174	hv.poly.2	0.3 min. spacing of hvPolyExmpt & unrelDiff
r1175	hv.poly.3	0.55 min. spacing of hvPolyExmpt2 & nwell
r1176	hv.poly.4	0.3 min. enclosure of hvPolyExmpt2 by nwell
r1177	hv.poly.6a	0.16 min extension of poly beyond hv gate is
r1178	hv.poly.6b	0.16 min extension of hvpoly beyond gate
r1179	x.22	Floating poly_float or poly_tie text not over poly
r1180	x.22	poly marked with poly_float not floating
r1181	x.22	Nets on poly is floating
r1182	x.22	Metal on poly is texted as both tied and floating (IP Level)
r1183	x.22	Floating li1_float or li1_tie text not over li1
r1184	x.22	li1 marked with li1_float not floating
r1185	x.22	Nets on li1 is floating
r1186	x.22	Metal on li1 is texted as both tied and floating (IP Level)
r1187	x.22	Floating m1_float or m1_tie text not over met1
r1188	x.22	met1 marked with m1_float not floating
r1189	x.22	Nets on met1 is floating
r1190	x.22	Metal on met1 is texted as both tied and floating (IP Level)
r1191	x.22	Floating m2_float or m2_tie text not over met2
r1192	x.22	met2 marked with m2_float not floating
r1193	x.22	Nets on met2 is floating
r1194	x.22	Metal on met2 is texted as both tied and floating (IP Level)
r1195	x.22	Floating m3_float or m3_tie text not over met3
r1196	x.22	met3 marked with m3_float not floating
r1197	x.22	Nets on met3 is floating
r1198	x.22	Metal on met3 is texted as both tied and floating (IP Level)
r1199	x.22	Floating m4_float or m4_tie text not over met4
r1200	x.22	met4 marked with m4_float not floating
r1201	x.22	Nets on met4 is floating
r1202	x.22	Metal on met4 is texted as both tied and floating (IP Level)
r1203	x.22	Floating m5_float or m5_tie text not over met5

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ID	Name	Description
r1204	x.22	met5 marked with m5_float not floating
r1205	x.22	Nets on met5 is floating
r1206	x.22	Metal on met5 is texted as both tied and floating (IP Level)
r1207	x.24	condiode label must be in isolated pwell
r1208	pad.20	met1 shielding pad, must not float
r1209	pad.20	met1 shielding pad, must not connected to pad
r1210	m1.x.1	<70% metal density when 700x700 window 100% covered by mm1.waffledrop
r1211	m1.x.1	<65% metal density when 700x700 window 80-100% covered by mm1.waffledrop
r1212	m1.x.1	<60% metal density when 700x700 window 60-80% covered by mm1.waffledrop
r1213	m1.x.1	<50% metal density when 700x700 window 50-60% covered by mm1.waffledrop
r1214	m1.x.1	<40% metal density when 700x700 window 40-50% covered by mm1.waffledrop
r1215	m1.x.1	<30% metal density when 700x700 window 30-40% covered by mm1.waffledrop
r1216	m2.x.1	<70% metal density when 700x700 window 100% covered by mm2.waffledrop
r1217	m2.x.1	<65% metal density when 700x700 window 80-100% covered by mm2.waffledrop
r1218	m2.x.1	<60% metal density when 700x700 window 60-80% covered by mm2.waffledrop
r1219	m2.x.1	<50% metal density when 700x700 window 50-60% covered by mm2.waffledrop
r1220	m2.x.1	<40% metal density when 700x700 window 40-50% covered by mm2.waffledrop
r1221	m2.x.1	<30% metal density when 700x700 window 30-40% covered by mm2.waffledrop
r1222	m3.x.1	<70% metal density when 700x700 window 100% covered by mm3.waffledrop
r1223	m3.x.1	<65% metal density when 700x700 window 80-100% covered by mm3.waffledrop
r1224	m3.x.1	<60% metal density when 700x700 window 60-80% covered by mm3.waffledrop
r1225	m3.x.1	<50% metal density when 700x700 window 50-60% covered by mm3.waffledrop
r1226	m3.x.1	<40% metal density when 700x700 window 40-50% covered by mm3.waffledrop
r1227	m3.x.1	<30% metal density when 700x700 window 30-40% covered by mm3.waffledrop
r1228	m4.x.1	<70% metal density when 700x700 window 100% covered by mm4.waffledrop
r1229	m4.x.1	<65% metal density when 700x700 window 80-100% covered by mm4.waffledrop
r1230	m4.x.1	<60% metal density when 700x700 window 60-80% covered by mm4.waffledrop
r1231	m4.x.1	<50% metal density when 700x700 window 50-60% covered by mm4.waffledrop
r1232	m4.x.1	<40% metal density when 700x700 window 40-50% covered by mm4.waffledrop
r1233	m4.x.1	<30% metal density when 700x700 window 30-40% covered by mm4.waffledrop
r1234	met-blk.1	0.14 min. spacing of met1 & met1Block
r1235	met-blk.1	met1 must not overlap met1Block
r1236	met-blk.3	0.145 min. spacing of met1Block & met1Routing
r1237	met-blk.1	0.14 min. spacing of met2 & met2Block
r1238	met-blk.1	met2 must not overlap met2Block
r1239	met-blk.3	0.145 min. spacing of met2Block & met2Routing
r1240	met-blk.1	0.3 min. spacing of met3 & met3Block
r1241	met-blk.1	met3 must not overlap met3Block
r1242	met-blk.3	0.305 min. spacing of met3Block & met3Routing
r1243	met-blk.1	0.3 min. spacing of met4 & met4Block

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ID	Name	Description
r1244	met-blk.1	met4 must not overlap met4Block
r1245	met-blk.3	0.305 min. spacing of met4Block & met4Routing
r1246	met-blk.1	1.6 min. spacing of met5 & met5Block
r1247	met-blk.1	met5 must not overlap met5Block
r1248	met-blk.3	1.605 min. spacing of met5Block & met5Routing
r1249	met-blk.2	0.17 min. spacing of li1 & li1Block
r1250	met-blk.2	li1 must not overlap li1Block
r1251	met-blk.4	0.17 min. spacing of li1Block & li1Routing
r1252	met-blk.6	prBoundary.boundary not allowed in layout
r1253	met-blk.7	poly.boundary not allowed in layout
r1254	met-blk.7	diff.boundary not allowed in layout
r1255	met-blk.7	tap.boundary not allowed in layout
r1256	fomdmy.1	0.5 min. width of fomDummyDRC
r1257	fomdmy.1	max width of fom dummy 25.0
r1258	fomdmy.2	0.4 min. spacing/notch of fomDummyDRC
r1259	fomdmy.4	1 min. spacing of fomDummyDRC & SEALID
r1260	fomdmy.4	fomDummyDRC must not overlap SEALID
r1261	fomdmy.6	3.25 min. spacing of fomDummyDRC & fuse
r1262	fomdmy.6	fomDummyDRC must not overlap fuse
r1263	fomdmy.7	0.13 min. spacing of fomDummyDRC & nsdm
r1264	fomdmy.7	fomDummyDRC must not overlap nsdm
r1265	fomdmy.7	0.13 min. spacing of fomDummyDRC & psdm
r1266	fomdmy.7	fomDummyDRC must not overlap psdm
r1267	fomdmy.8	0.18 min. enclosure of fomDummyDRC by nwell
r1268	fomdmy.9	0.34 min. spacing of fomDummyDRC & nwell
r1269	fomdmy.10	0.43 min. enclosure of fomDummyDRC by HVnwell
r1270	fomdmy.1	0.33 min. spacing of fomDummyDRC & HVnwell
r1271	fomdmy.1	0.5 min. enclosure of fomDummyDRC by FRAMEID
r1272	fomdmy.1	0.5 min. spacing of fomDummyDRC & dieCut
r1273	rdl.1	10 min. width of rdl
r1274	rdl.2	10 min. spacing/notch of rdl
r1275	rdl.2	10 min. spacing/notch of rdl
r1276	rdl.3	10.75 min. enclosure of pad by nonCSPRDL
r1277	rdl.4	15 min. enclosure of rdl by SEALnoHoles_ORIGIN
r1278	rdl.5	(rdl OR ccu1m.mk) in scribe must not overlap areaid.ft.
r1279	rdl.6	19.66 min. spacing of nonCSPRDL & pad
r1280	mf.1&2	metal4 fuse should be rectangular
r1281	mf.1&2	0.8 min. width of metal4 fuse

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ID	Name	Description
r1282	mf.1&2	0.8 max. width of metal4 fuse
r1283	mf.1&2	7.2 min. length of metal4 fuse
r1284	mf.1&2	7.2 max. length of metal4 fuse
r1285	mf.3	2.75 min. spacing of target
r1286	mf.5	0.83 max extension of met4 beyond fuse boundary
r1287	mf.22	1.96 min. spacing of METxContact
r1288	mf.6	3.295 min. spacing of target & met1
r1289	mf.6	target must not overlap met1
r1290	mf.7	3.295 min. spacing of target & li1
r1291	mf.7	target must not overlap li1
r1292	mf.8	2.655 min. spacing of target & poly
r1293	mf.8	target must not overlap poly
r1294	mf.9	2.635 min. spacing of target & tap
r1295	mf.9	target must not overlap tap
r1296	mf.10	3.245 min. spacing of target & diff
r1297	mf.10	target must not overlap diff
r1298	mf.11	3.315 min. spacing of target & nwell
r1299	mf.11	target must not overlap nwell
r1300	mf.19	3.295 min. spacing of target & met2
r1301	mf.19	target must not overlap met2
r1302	mf.12	mf.12: 2.40x0.50 size of a fuse_shield
r1303	mf.4	3.295 min. spacing of target & METnotFUSE
r1304	mf.13	2.195 min. spacing of target & fuseShield
r1305	mf.14	max shield to target spacing
r1306	mf.15a	fuseShield is allowed for non_isolated fuse edges ONLY
r1307	mf.15b	fuseShield is required between peri metal and non isolated fuse edges
r1308	mf.18	0.6 min&max space between fuse_shield and met4
r1309	mf.20	only one fuse allowed per metal line
r1310	mf.24	3.295 min. spacing of target & met5
r1311	mf.24	target must not overlap met5
r1312	pad.1	padPL pcells should be used for bondpad
r1313	pad.1	padPL pcells should have text plastic to be used for bondpad
r1314	pad.16	Hermetic package pads are not supported inthis flow
r1315	pad.4/4a	2.7 min. enclosure of bondpadNormal by met5
r1316	pad.5	Zero Spacing between lower level met4 ring and Advanced Bondpad
r1317	pad.6	5 min. spacing of smallGroupingY & met5OutsidePad
r1318	pad.7	10 min. spacing of largeGroupingY & met5OutsidePad
r1319	pad.6	5 min. spacing of smallGroupingX & met5OutsidePad
r1320	pad.7	10 min. spacing of largeGroupingX & met5OutsidePad
r1321	pad.6	5 min. spacing of smallGroupingY & met4OutsidePad
r1322	pad.7	10 min. spacing of largeGroupingY & met4OutsidePad
r1323	pad.6	5 min. spacing of smallGroupingX & met4OutsidePad
r1324	pad.7	10 min. spacing of largeGroupingX & met4OutsidePad
r1325	pad.10	bondpadNormalNoprobe must not overlap met4
r1326	pad.11	Bondpad should not have 90 degree corner
r1327	pad.11	Bondpad should have 45 degree corner
r1328	pad.11	Bondpad should have only 4 45 degree corner
r1329	pad.11	Bondpad should have only 4 orthogonal edges
r1330	pad.12	7.0 Min length of 45 degree bevel on Bond pad
r1331	pad.13	8.8 Max length of 45 degree bevel on Bond pad

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ID	Name	Description
r1332	pad.14	16.99 min. enclosure of anyPadPlastic by solid_seal
r1333	pad.15	500.0 Max spacing between bondpad opening and edge of scribe line(outer end of seal ring)
r1334	pad.17	1.5 min. spacing/notch of met1UndPadMetOnly
r1335	pad.18	0.14 min width of met1 under pad metal
r1336	pad.17	1.5 min. spacing/notch of met2UndPadMetOnly
r1337	pad.18	0.14 min width of met2 under pad metal
r1338	pad.17	1.5 min. spacing/notch of met3UndPadMetOnly
r1339	pad.18	0.3 min width of met3 under pad metal
r1340	pad.19	25 max width of met1 under pad metal
r1341	pad.19	25 max width of met2 under pad metal
r1342	pad.19	6 max width of met3 under pad metal
r1343	pad.2.1	60 min width of padPLFP in x direction
r1344	pad.3.1	60 min length of padPLFP in y direction
r1345	pad.4.1	60 min width of padPLSTG in x direction
r1346	pad.5.1	60 min length of padPLSTG in y direction
r1347	pad.6.1	60 min width of padPLHP in x direction
r1348	pad.6.1	60 min length of padPLHP in y direction
r1349	pad.6.1a	58 min width of padPLHPcu in x direction
r1350	pad.6.1b	60 min length of padPLHPcu in y direction
r1351	pad.6.1a/b	58x60 min dimensions of padPLHPcu which are not within 50 of other pad
r1352	pad.7.1	50 min width of padPLWLBI in x direction
r1353	pad.8.1	60 min length of padPLWLBI in y direction
r1354	pad.2/3.1	bondpadCuPillarSz should be rectangular
r1355	pad.2/3.1	39 min. width of bondpadCuPillarSz
r1356	pad.2/3.1	39 max. length of bondpadCuPillarSz
r1357	pad.1.2	8 min space of padPLFP in x direction to padPLFP/HP/STG/WLBI
r1358	pad.2.2	15 min space of padPLHPorg in x direction to padPLHP/STG/WLBI
r1359	pad.2.2a	7 min space of padPLHPcu in x direction to padPLHPcu/STG/WLBI
r1360	pad.3.2	50 min space of padPLWLBI in x direction to padPLSTG/WLBI
r1361	pad.4.2	30 min space of padPLSTG in x direction to padPLSTG
r1362	pad.9.1	150.0um Max Width/Length of bond pad
r1363	pad.6.2	39.8 min. spacing of padCenterSTGinDieXy
r1364	pad.6.2	39.8 min. spacing of padCenterSTGinDieYy
r1365	pad.5.2.4	9 min. spacing of padSTGinDieXsp & bondPadSTG
r1366	pad.7.2.1	284 min space of padPLSTG in x direction to adjacent scribe
r1367	pad.7.2.2	200 min space of padPLFP in x direction to adjacent scribe
r1368	pad.7.2.2	200 min space of padPLWLBI in x direction to adjacent scribe
r1369	cupad.1	5 min. width of pad opening inside inductor
r1370	cupad.2	0 min. enclosure of pad opening inside inductor by pmm
r1371	cupad.2	pad opening inside inductor must be enclosed by pmm
r1372	cupad.3	2.7 min. enclosure of pad opening inside inductor by met5
r1373	cupad.3	pad opening inside inductor must be enclosed by met5
r1374	cupad.4	10.75 min. enclosure of pmm inside inductor by rdl
r1375	cupad.4	pmm inside inductor must be enclosed by rdl
r1376	scribe.5	Wide diff >= 10.0x10.0um within 150.0 of scribe junction
r1377	scribe.5	Wide poly >= 10.0x10.0um within 150.0 of scribe junction
r1378	scribe.5	Wide li1 >= 10.0x10.0um within 150.0 of scribe junction
r1379	scribe.5	Wide met1 >= 10.0x10.0um within 150.0 of scribe junction
r1380	scribe.5	Wide met2 >= 10.0x10.0um within 150.0 of scribe junction
r1381	scribe.5	Wide met3 >= 10.0x10.0um within 150.0 of scribe junction

Table 5.96 – continued from previous page

ID	Name	Description
r1382	scribe.5	Wide mcon >= 10.0x10.0um within 150.0 of scribe junction
r1383	scribe.5	Wide licon1 >= 10.0x10.0um within 150.0 of scribe junction
r1384	scribe.5	Wide via >= 10.0x10.0um within 150.0 of scribe junction
r1385	scribe.5	Wide via2 >= 10.0x10.0um within 150.0 of scribe junction
r1386	scribe.5	Wide met4 >= 10.0x10.0um within 150.0 of scribe junction
r1387	scribe.5	Wide met5 >= 10.0x10.0um within 150.0 of scribe junction
r1388	scribe.5	Wide via3 >= 10.0x10.0um within 150.0 of scribe junction
r1389	scribe.5	Wide via4 >= 10.0x10.0um within 150.0 of scribe junction
r1390	scribe.5	Wide mm1mk >= 10.0x10.0um within 150.0 of scribe junction
r1391	scribe.5	Wide mm2mk >= 10.0x10.0um within 150.0 of scribe junction
r1392	scribe.5	Wide mm3mk >= 10.0x10.0um within 150.0 of scribe junction
r1393	scribe.5	Wide p1mmk >= 10.0x10.0um within 150.0 of scribe junction
r1394	scribe.5	Wide fommk >= 10.0x10.0um within 150.0 of scribe junction
r1395	scribe.5	Wide ctm1mk >= 10.0x10.0um within 150.0 of scribe junction
r1396	scribe.5	Wide licm1mk >= 10.0x10.0um within 150.0 of scribe junction
r1397	scribe.5	Wide li1mmk >= 10.0x10.0um within 150.0 of scribe junction
r1398	scribe.5	Wide vimmk >= 10.0x10.0um within 150.0 of scribe junction
r1399	scribe.5	Wide vim2mk >= 10.0x10.0um within 150.0 of scribe junction
r1400	scribe.5	Wide mm4mk >= 10.0x10.0um within 150.0 of scribe junction
r1401	scribe.5	Wide mm5mk >= 10.0x10.0um within 150.0 of scribe junction
r1402	scribe.5	Wide vim3mk >= 10.0x10.0um within 150.0 of scribe junction
r1403	scribe.5	Wide vim4mk >= 10.0x10.0um within 150.0 of scribe junction
r1404	scribe.6a	pad inside frame or moduleCut without text label
r1405	scribe.6d	mconOrVia must not overlap EUTESTPAD
r1406	scribe.6e	EUTESTPAD must be enclosed by areaid module cut AND areaid etest
r1407	scribe.7	nwell drawn layer cannot straddle areaid:ModuleCut
r1408	scribe.7	diff drawn layer cannot straddle areaid:ModuleCut
r1409	scribe.7	dnwell drawn layer cannot straddle areaid:ModuleCut
r1410	scribe.7	tap drawn layer cannot straddle areaid:ModuleCut
r1411	scribe.7	lvtn drawn layer cannot straddle areaid:ModuleCut
r1412	scribe.7	hvtp drawn layer cannot straddle areaid:ModuleCut
r1413	scribe.7	hvi drawn layer cannot straddle areaid:ModuleCut
r1414	scribe.7	tunm drawn layer cannot straddle areaid:ModuleCut
r1415	scribe.7	poly drawn layer cannot straddle areaid:ModuleCut
r1416	scribe.7	npc drawn layer cannot straddle areaid:ModuleCut
r1417	scribe.7	nsdm drawn layer cannot straddle areaid:ModuleCut
r1418	scribe.7	psdm drawn layer cannot straddle areaid:ModuleCut
r1419	scribe.7	licon1 drawn layer cannot straddle areaid:ModuleCut
r1420	scribe.7	li1 drawn layer cannot straddle areaid:ModuleCut
r1421	scribe.7	mcon drawn layer cannot straddle areaid:ModuleCut
r1422	scribe.7	met1 drawn layer cannot straddle areaid:ModuleCut
r1423	scribe.7	via drawn layer cannot straddle areaid:ModuleCut
r1424	scribe.7	met2 drawn layer cannot straddle areaid:ModuleCut
r1425	scribe.7	vhvi drawn layer cannot straddle areaid:ModuleCut
r1426	scribe.7	via2 drawn layer cannot straddle areaid:ModuleCut
r1427	scribe.7	met3 drawn layer cannot straddle areaid:ModuleCut
r1428	scribe.7	via3 drawn layer cannot straddle areaid:ModuleCut
r1429	scribe.7	met4 drawn layer cannot straddle areaid:ModuleCut
r1430	scribe.7	via4 drawn layer cannot straddle areaid:ModuleCut
r1431	scribe.7	met5 drawn layer cannot straddle areaid:ModuleCut

Table 5.96 – continued from previous page

ID	Name	Description
r1432	scribe.7	nsm drawn layer cannot straddle areaid:ModuleCut
r1433	scribe.7	pad drawn layer cannot straddle areaid:ModuleCut
r1434	scribe.7	ldntm drawn layer cannot straddle areaid:ModuleCut
r1435	scribe.7	hvntm drawn layer cannot straddle areaid:ModuleCut
r1436	scribe.7	pmm drawn layer cannot straddle areaid:ModuleCut
r1437	scribe.7	pnp drawn layer cannot straddle areaid:ModuleCut
r1438	scribe.7	capacitor drawn layer cannot straddle areaid:ModuleCut
r1439	scribe.7	ncm drawn layer cannot straddle areaid:ModuleCut
r1440	scribe.7	pmm2 drawn layer cannot straddle areaid:ModuleCut
r1441	scribe.7	inductor drawn layer cannot straddle areaid:ModuleCut
r1442	scribe.7	rdl drawn layer cannot straddle areaid:ModuleCut
r1443	scribe.7	rpm drawn layer cannot straddle areaid:ModuleCut
r1444	scribe.7	hvtr drawn layer cannot straddle areaid:ModuleCut
r1445	scribe.7	ubm drawn layer cannot straddle areaid:ModuleCut
r1446	scribe.7	bump drawn layer cannot straddle areaid:ModuleCut
r1447	scribe.8	Etest-pad-67 and Etest-pad-35 should not exist in the same module
r1448	scribe.9	Etest pad Width and Length is either 67.00 um or 35.00um
r1449	scribe.10	Min/Max Spacing between Etest pad (67um*67um) with in same module should be 90.5um
r1450	scribe.10	Min/MaxSpacing between Etest pad (67um*67um)with in same module should be 90.5um
r1451	scribe.11	Min/Max Spacing between Etest pad (35um*35um) with in same module should be 55um
r1452	scribe.11	Min/MaxSpacing between Etest pad (35um*35um)with in same module should be 55um
r1453	scribe.12	7.5 min. enclosure of ETESTPAD by areaid module cut
r1454	scribe.13	2.50um min. enclosure of Etest pad by met1
r1455	scribe.13	2.5 min. enclosure of ETESTPAD_met1 by met1
r1456	scribe.13	2.50um min. enclosure of Etest pad by met2
r1457	scribe.13	2.5 min. enclosure of ETESTPAD_met2 by met2
r1458	scribe.13	2.50um min. enclosure of Etest pad by met3
r1459	scribe.13	2.5 min. enclosure of ETESTPAD_met3 by met3
r1460	scribe.13	2.50um min. enclosure of Etest pad by met4
r1461	scribe.13	2.5 min. enclosure of ETESTPAD_met4 by met4
r1462	scribe.13	2.50um min. enclosure of Etest pad by met5
r1463	scribe.13	2.5 min. enclosure of ETESTPAD_met5 by met5
r1464	scribe.14	Minimum Utest pad Width and Length is 10um
r1465	scribe.15	Min Spacing between Utest pad opening should be 15um
r1466	scribe.16	Min Spacing between Utest pad and Etest pad opening should be 7um
r1467	scribe.17	2.5 min. enclosure of UTESTPAD by met5
r1468	scribe.18	Spacing of E-test pad opening to E-test pad opening in the same module must all be equal
r1469	scribe.18	Spacing of E-test pad opening to E-test pad opening in the same module must all be equal
r1470	scribe.19	76 min. width of realScribeLine
r1471	scribe.20	Pad.dg is to be drawn from 3.0um from scribe edge to 13.0um from scribe edge
r1472	scribe.21	Scribe must not enclose pdm.dg nor pdm.mk except for etest pads, die pad rings
r1473	chvtpm.1	0.38 min. width of CLHVTPM
r1474	chvtpm.2a	0.38 min. spacing/notch of CLHVTPM
r1475	chvtpm.3	0 min. enclosure of ((LVnwell not overlapping Var_channel) NOT lvtn) by CLHVTPM
r1476	chvtpm.4	0 min. enclosure of ((LVnwell overlapping Var_channel) AND hvtp) by CLHVTPM
r1477	clvtnm.1	0.38 min. width of clvtnm in periphery
r1478	clvtnm.2	0.38 min. spacing/notch of CLLVTNM
r1479	cntm.2	0.7 min. spacing/notch of CLNTM
r1480	cntm.1	0.84 min. width of CLNTM
r1481	cntm.3	0 min. enclosure of nwell by CLNTM

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ID	Name	Description
r1482	cntm.3	nwell must be enclosed by CLNTM
r1483	cntm.4a	0 min. enclosure of hvitmp by CLNTM
r1484	cntm.4a	hvitmp must be enclosed by CLNTM
r1485	cntm.7	0 min. enclosure of ldntm by CLNTM
r1486	cntm.7	ldntm must be enclosed by CLNTM
r1487	chvntm.1	0.7 min. width of CLHVNTM
r1488	chvntm.2a	0.7 min. spacing/notch of CLHVNTM
r1489	chvntm.4	0.185 min. spacing of CLHVNTM & NDIFFnoHV
r1490	chvntm.4	CLHVNTM must not overlap NDIFFnoHV
r1491	chvntm.5	0.185 min. spacing of CLHVNTM & PDIFF_noENID
r1492	chvntm.5	CLHVNTM must not overlap PDIFF_noENID
r1493	chvntm.3	0.185 Min Enclosure of ndiff inside hvi by chvntm
r1494	chvntm.6a	0.185 min. spacing of CLHVNTM & p+tap (except along the diff butting edge)
r1495	chvntm.6a	CLHVNTM must not overlap ptap
r1496	chvntm.6b	CLHVNTM must not overlap p+diff along diff butting edge (ESDnWellTap excluded)
r1497	chvntm.7	ESDnWellTapHV must be enclosed by CLHVNTM
s0	x.18	single mcon_NOTAreaidStdCellCore that can be doubled
s1	x.18	single via_NOTAreaidStdCellCore that can be doubled
s2	x.18	single via2_NOTAreaidStdCellCore that can be doubled
s3	x.18	single via3_NOTAreaidStdCellCore that can be doubled
s4	x.18	single via4_NOTAreaidStdCellCore that can be doubled
s5	x.23f	ptap must not straddle localSub
s6	x.27	partnum or partnum exclusion 'partnum_not_necessary' not present on chip
s7	x.27	partnum*block pcell should be used instead of partnum* pcells
s8	m2.3c	Crater: spacing matches between met2 areas with via2-to-SurfaceArea ratio >=0.05 and =< 0.032
s9	x.22	Floating poly_float or poly_tie text not over poly
s10	x.22	poly marked with poly_float not floating
s11	x.22	Nets on poly is floating
s12	x.22	Floating poly marked with poly_tie at chiplevel without connecting
s13	x.22	Metal on poly is texted as both tied and floating (Chip level)
s14	x.22	Floating li1_float or li1_tie text not over li1
s15	x.22	li1 marked with li1_float not floating
s16	x.22	Nets on li1 is floating
s17	x.22	Floating li1 marked with li1_tie at chiplevel without connecting
s18	x.22	Metal on li1 is texted as both tied and floating (Chip level)
s19	x.22	Floating m1_float or m1_tie text not over met1
s20	x.22	met1 marked with m1_float not floating
s21	x.22	Nets on met1 is floating
s22	x.22	Floating met1 marked with m1_tie at chiplevel without connecting
s23	x.22	Metal on met1 is texted as both tied and floating (Chip level)
s24	x.22	Floating m2_float or m2_tie text not over met2
s25	x.22	met2 marked with m2_float not floating
s26	x.22	Nets on met2 is floating
s27	x.22	Floating met2 marked with m2_tie at chiplevel without connecting
s28	x.22	Metal on met2 is texted as both tied and floating (Chip level)
s29	x.22	Floating m3_float or m3_tie text not over met3
s30	x.22	met3 marked with m3_float not floating
s31	x.22	Nets on met3 is floating
s32	x.22	Floating met3 marked with m3_tie at chiplevel without connecting

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Table 5.96 – continued from previous page

ID	Name	Description
s33	x.22	Metal on met3 is texted as both tied and floating (Chip level)
s34	x.22	Floating m4_float or m4_tie text not over met4
s35	x.22	met4 marked with m4_float not floating
s36	x.22	Nets on met4 is floating
s37	x.22	Floating met4 marked with m4_tie at chiplevel without connecting
s38	x.22	Metal on met4 is texted as both tied and floating (Chip level)
s39	x.22	Floating m5_float or m5_tie text not over met5
s40	x.22	met5 marked with m5_float not floating
s41	x.22	Nets on met5 is floating
s42	x.22	Floating met5 marked with m5_tie at chiplevel without connecting
s43	x.22	Metal on met5 is texted as both tied and floating (Chip level)
s44	m1.x.1	<70% metal density when 700x700 window 100% covered by mm1.waffledrop
s45	m1.x.1	<65% metal density when 700x700 window 80-100% covered by mm1.waffledrop
s46	m1.x.1	<60% metal density when 700x700 window 60-80% covered by mm1.waffledrop
s47	m1.x.1	<50% metal density when 700x700 window 50-60% covered by mm1.waffledrop
s48	m1.x.1	<40% metal density when 700x700 window 40-50% covered by mm1.waffledrop
s49	m1.x.1	<30% metal density when 700x700 window 30-40% covered by mm1.waffledrop
s50	m2.x.1	<70% metal density when 700x700 window 100% covered by mm2.waffledrop
s51	m2.x.1	<65% metal density when 700x700 window 80-100% covered by mm2.waffledrop
s52	m2.x.1	<60% metal density when 700x700 window 60-80% covered by mm2.waffledrop
s53	m2.x.1	<50% metal density when 700x700 window 50-60% covered by mm2.waffledrop
s54	m2.x.1	<40% metal density when 700x700 window 40-50% covered by mm2.waffledrop
s55	m2.x.1	<30% metal density when 700x700 window 30-40% covered by mm2.waffledrop
s56	m3.x.1	<70% metal density when 700x700 window 100% covered by mm3.waffledrop
s57	m3.x.1	<65% metal density when 700x700 window 80-100% covered by mm3.waffledrop
s58	m3.x.1	<60% metal density when 700x700 window 60-80% covered by mm3.waffledrop
s59	m3.x.1	<50% metal density when 700x700 window 50-60% covered by mm3.waffledrop
s60	m3.x.1	<40% metal density when 700x700 window 40-50% covered by mm3.waffledrop
s61	m3.x.1	<30% metal density when 700x700 window 30-40% covered by mm3.waffledrop
s62	m4.x.1	<70% metal density when 700x700 window 100% covered by mm4.waffledrop
s63	m4.x.1	<65% metal density when 700x700 window 80-100% covered by mm4.waffledrop
s64	m4.x.1	<60% metal density when 700x700 window 60-80% covered by mm4.waffledrop
s65	m4.x.1	<50% metal density when 700x700 window 50-60% covered by mm4.waffledrop
s66	m4.x.1	<40% metal density when 700x700 window 40-50% covered by mm4.waffledrop
s67	m4.x.1	<30% metal density when 700x700 window 30-40% covered by mm4.waffledrop
s68	met-blk.6	prBoundary.boundary not allowed in layout
s69	met-blk.7	poly.boundary not allowed in layout
s70	met-blk.7	diff.boundary not allowed in layout
s71	met-blk.7	tap.boundary not allowed in layout
s72	chip-int.1	areaid.ld not allowed within 50.0 um of ESDID
s73	chip-int.2	areaid.ij not allowed within 150.0 um of ESDID

SIX

PDK CONTENTS

6.1 Libraries

6.1.1 Library Naming

Libraries in the SKY130 PDK are named using the following scheme;

<Process name> _ <Library Source Abbreviation> _ <Library Type Abbreviation> [_ <Library Name>]

All sections are **lower case** and separated by an **underscore**. The sections are;

- The Process name in is the name of the process technology, for this PDK it is always sky130.

- The Library Source Abbreviations is a short abbreviation for who created and is responsible for the library. The table below shows the current list of Library Source Abbreviations;

Library Source	Library Source Abbreviation
The SkyWater Foundry	fd
Efabless	ef
Oklahoma State University	osu

- The Library Type Abbreviation is a short two letter abbreviation for the type of content found in the library. The table below shows the current list of Library Type Abbreviations;

Library Type	Library Type Abbreviation
Primitive Cells	pr
Digital Standard Cells	sc
Build Space (Flash, SRAM, etc)	bd
IO and Periphery	io
Miscellaneous	xx

- The Library Name is an optional short abbreviated name used when there are multiple libraries of a given type released from a single library source. If only one library of a given type is going to ever be released, this can be left out.

6.1.2 Creating New Libraries

Third party developers are encourage to create new and interesting libraries for usage with the SKY130 process technology. These libraries can even be included in the SKY130 PDK if it meets the following criteria;

- It is released under an OSI approved license.

- TODO: Finish the criteria.

6.1.3 Primitive Libraries

Foundry provided

6.1.4 Digital Standard Cell Libraries

Foundry provided Digital Standard Cell Libraries

SkyWater Foundry Provided Standard Cell Libraries

There are seven standard cell libraries provided directly by the SkyWater Technology foundry available for use on SKY130 designs, which differ in intended applications and come in three separate cell heights.

Libraries sky130_fd_sc_hs (high speed), sky130_fd_sc_ms (medium speed), sky130_fd_sc_ls (low speed), and sky130_fd_sc_lp (low power) are compatible in size, with a 0.48 x 3.33um site, equivalent to about 11 met1 tracks.

Libraries sky130_fd_sc_hd (high density) and sky130_fd_sc_hdll (high density, low leakage) contain standard cells that are smaller, utilizing a 0.46 x 2.72um site, equivalent to 9 met1 tracks.

The sky130_fd_sc_hvl (high voltage) library contains 5V devices and utilizes a 0.48 x 4.07um site, or 14 met1 tracks.

Supply voltage, FETs, and approximate cell counts for these libraries appear in the table below:

	sky130_fd_	sky130_fd_	sky130_fd_	sky130_fd_	sky130_fd	sky130_fd_	sky130_fd_sc_hvl
VDD	1.8	1.8	1.8	1.8	1.8	1.8	5
NMOS devices used	sky130_fd_p	sky130_fd_p	sky130_fd_p	sky130_fd_p	sky130_fd_	sky130_fd_p	sky130_fd_pr__nfet_g5v0d10v5
PMOS devices used	sky130_fd_p	sky130_fd_p	sky130_fd_p	sky130_fd_p	sky130_fd_	sky130_fd_p	sky130_fd_pnvtpfet_g5v0d10v5
inverters, buffers	108	48	48	48	56	62	19
AND, OR, NAND, NOR	159	66	86	86	153	170	8
XOR, XNOR	16	12	12	12	8	10	2
AND-OR-INV, OR-AND-INV	138	71	71	71	115	125	4
AND-OR, OR-AND	132	68	68	68	132	134	4
Adders, Comparators, Multiplexors	59	37	33	33	31	44	11
Latches and Flip-Flops	92	68	68	68	60	60	17
Custom power gating, bus cells	43	66	42	42	51	42	
Macro cells		5					
UDB custom cells		21	17				

The libraries uses 4 terminal transistors throughout. Individual cells do not have tap in them for the most part (there are a few exceptions). Instead, there are tap cells provided that allow for a staggered tap grid to be placed and connected to allow for body biasing, sleep mode support, and latchup protection.

The following sections will review the libraries in more detail, in terms of performance.

Architecture Comparison	Low Speed	High Density	High Density Low Leakage	High Voltage
TAP BAR	NO	NO	NO	YES
X-GRID	0.480	0.460	0.460	0.480
Y-GRID	0.370	0.340	0.340	0.370
CELL HEIGHT	9 GRIDS	8 GRIDS	8 GRIDS	11 GRIDS
CELL HEIGHT	3.330	2.720	2.720	4.07
NAND2 WIDTH	3 GRIDS	3 GRIDS	4 GRIDS	5 GRIDS
NAND2 WIDTH	1.440	1.380	1.840	2.400
NAND2 AREA	4.7952	3.7536	5.0048	9.770
WPMAX	1.120	1.000	1.000	1.500
WNMAX	0.740	0.650	0.650	0.75

sky130_fd_sc_hd - High Density Standard Cell Library

The sky130_fd_sc_hd library is designed for high density.

Compared to sky130_fd_sc_ls, this library enables higher routed gated density, lower dynamic power consumption, and comparable timing and leakage power. As a trade-off it has lower drive strength and does not support any drop in replacement medium or high speed library.

- sky130_fd_sc_hd includes clock-gating cells to reduce active power during non-sleep modes.

- Latches and flip-flops have scan equivalents to enable scan chain creation.

- Multi-voltage domain library cells are provided.

- Routed Gate Density is 160 kGates/mm^2 or better.

- leakage @ttleak_1.80v_25C (no body bias) is 0.86 nA / kGate

- sky130_fd_sc_XX__buf_16 max cap (ss_1.60v_-40C, in/out tran=1.5ns) is 0.746 pF

- Body Bias-able

sky130_fd_sc_hdll - High Density, Low Leakage Standard Cell Library

The sky130_fd_sc_hdll library is a low leakage high density standard cell library.

Compared to sky130_fd_sc_hd, this library enables 5-10X lower leakage power, but the same X, Y pin grids, routing layer pitches, and cell height.

Blocks should be DRC clean when intermingled with sky130_fd_sc_hd cells.

Raw gate density (number of sky130_fd_sc_hdll__nand2_1 gates able to fit in 1mm2) for sky130_fd_sc_hd is 266kGates/mm2 and 200kGates/mm2 for sky130_fd_sc_hdll.

- Includes integrating clock-gating cells to reduce active power during non-sleep modes

- Latches and flip-flops in the library have a scan equivalent implementation to enable scan chain creation and testing supported by the synthesis tools

- Multi-voltage domain library cells are provided

- Routed Gate Density is 120 kGates/mm^2

- leakage @ttleak_1.80v_25C (no body bias) is 0.08 nA / kGate

- sky130_fd_sc_XX__buf_16 max cap (ss_1.60v_-40C, in/out tran=1.5ns) < 1 pF

- Multi-Voltage Design Support

- Body Bias-able

sky130_fd_sc_hs - Low Voltage (<2.0V), High Speed, Standard Cell Library

sky130_fd_sc_hs library enables the implementation of low voltage high speed logic blocks in the SKY130 technology.

sky130_fd_sc_hs cells are drop-in compatible with sky130_fd_sc_ms`a for the same function and drive strength. sky130_fd_sc_hs has the highest speed and the highest leakage of these.

All logic cells are implemented with low voltage transistors and should be powered within the limits of those transistors. Specifically, the timing and power models are valid from 1.60V up to 1.95V, with timing data included for 10% and 20% dynamic IR drop analysis.

All cells are functional at 1.2v. The low to high level shifter cells are capable of shifting from 1.2v to 1.95v.

sky130_fd_sc_ms - Low Voltage (<2.0V), Medium Speed, Standard Cell Library

sky130_fd_sc_ms is drop-in compatible with sky130_fd_sc_ls or sky130_fd_sc_hs libraries for cells of the same function and drive strength. sky130_fd_sc_ms cells have medium speed and leakage.

sky130_fd_sc_ms is implemented with low voltage transistors; timing and power models are valid from 1.60V up to 1.95V. All cells are functional at 1.2v.

The low to high level shifter cells are capable of shifting from 1.2v to 1.95v.

- The library supports low leakage sleep mode via state retention flops

- Includes integrating clock-gating cells to reduce active power during non-sleep modes

- Latches and flip-flops in the library have a scan equivalent implementation to enable scan chain creation and testing supported by the synthesis tools

- Library details:

    - Inverters and buffers: 48

    - AND, OR, NAND, NOR gates: 86

    - Exclusive-OR and Exclusive-NOR: 12

    - Inverted And-Or and Inverted Or-And: 71

    - And-Or and Or-And: 68

    - Adders, Comparators and Multiplexers: 33

    - Latches and filp-flops: 68

    - Low Power Flow Cells: 42

    - UDB custom cells: 17

sky130_fd_sc_ls - Low Voltage (<2.0V), Low Speed, Standard Cell Library

sky130_fd_sc_ls cells are drop-in compatible with sky130_fd_sc_ms`a for the same function and drive strength. sky130_fd_sc_ls has the lowest speed and the lowest leakage of these.

sky130_fd_sc_ls is implemented with low voltage transistors; timing and power models are valid from 1.60V up to 1.95V. All cells are functional at 1.2v.

The low to high level shifter cells are capable of shifting from 1.2v to 1.95v.

- The library supports low leakage sleep mode via sleep transistors

- Includes integrating clock-gating cells to reduce active power during non-sleep modes

- Latches and flip-flops in the library have a scan equivalent implementation to enable scan chain creation and testing supported by the synthesis tools

- Drop-in compatible with sky130_fd_sc_ms and sky130_fd_sc_hs libraries

- Only the high to low level-shifters are functional at 1v (sky130_fd_sc_ls__lpflow_lsbuf_hl_*). The low to high level-shifters (sky130_fd_sc_ls__lpflow_lsbuf_lh_*) are not functional at 1v as the threshold voltages of the FETs are not enough to flip the state.

- Library details:

    - Inverters and buffers: 48

    - AND, OR, NAND, NOR gates: 86

- Exclusive-OR and Exclusive-NOR: 12

- Inverted And-Or and Inverted Or-And: 71

- And-Or and Or-And: 68

- Adders, Comparators and Multiplexers: 37

- Latches and filp-flops: 68

- Low Power Flow Cells: 66

- Macro Cells: 5

- UDB Custom Cells: 21

sky130_fd_sc_lp - Low Voltage (<2.0V), Low Power, Standard Cell Library

sky130_fd_sc_lp is the largest of the SKY130 standard cell libraries at nearly 750 cells. All logic cells are implemented with low voltage transistors and should be powered within the limits of those transistors. Specifically, the timing and power models are valid from 1.55V up to 2.0V.

- sky130_fd_sc_lp supports low leakage sleep mode via sleep transistors

- Includes integrating clock-gating cells to reduce active power during non-sleep modes

- Latches and flip-flops have scan equivalents to enable scan chain creation

- Larger Library size:

  - Inverters, Buffers: 108

  - AND, OR, NAND, NOR gates: 159

  - Exclusive-OR, Exclusive-NOR: 16

  - AND-OR-Inverted, OR-AND-Inverted: 138

  - AND-OR, OR-AND: 132

  - Adders, Comparators, Multiplexors: 59

  - Custom Power gating, bus cells: 43

  - Latches and flip-flops: 92

sky130_fd_sc_hvl - High Voltage (5V), Standard Cell Library

The sky130_fd_sc_hvl library has the smallest cell count of the SKY130 standard cell libraries, but is the only one that enables 5V tolerant logic blocks. All logic cells are implemented with 5v tolerant transistors; timing and power models are valid from 1.65v to 5.5v. The low voltage to high voltage level shifter is functional shifting from 1.2v to 5.5v.

Raw gate density (number of sky130_fd_sc_hvl__nand2_1 gates able to fit in 1mm2) should be 170kGates/mm2.

Routed should be >= 100kGates/mm2. Due to the gate length for these high voltage transistors, the actual gate density is lower than 170kGates/mm2. The size of a 2-input NAND gate in this library is actually 5 grids wide, whereas the 170k calculation is based on a gate that is 3 grids wide. With a 5 grid wide gate, the raw gate density is 102kGates/mm2.

sky130_fd_sc_hd - SKY130 High Density Digital Standard Cells (SkyWater Provided)

Initial release of version (0, 0, 2).

sky130_fd_sc_hdll - SKY130 High Density Low Leakage Digital Standard Cells (SkyWater Provided)

Initial release of version (0, 1, 1).

sky130_fd_sc_hs - SKY130 High Speed Digital Standard Cells (SkyWater Provided)

Initial release of version (0, 0, 1).

sky130_fd_sc_ls - SKY130 Low Speed Digital Standard Cells (SkyWater Provided)

Initial release of version (0, 1, 1).

sky130_fd_sc_ms - SKY130 Medium Speed Digital Standard Cells (SkyWater Provided)

Initial release of version (0, 0, 1).

Third party provided Digital Standard Cell Libraries

6.1.5 Build Space Libraries

The SKY130 currently offers two build space libraries. Build space libraries are designed to be used with technologies like memory compilers and built into larger macros. The provided libraries have specially crafted design rules to enable higher density compared to other libraries.

Foundry provided Build Space Libraries

6.1.6 IO and Periphery Libraries

Foundry provided IO and Periphery Libraries

sky130_fd_io - SKY130 IO and periphery cells (SkyWater Provided)

Initial documentation only release.

User Guide for sky130_fd_io

Summary

Todo: sky130_fd_io__gpio is not yet publicly available.

This IP document includes two versions of a General Purpose I/O buffer (sky130_fd_io__gpio) with different feature sets, sky130_fd_io__sio macro (pair of Special I/O buffer (sky130_fd_io__sio) + REFerence GENerator (sky130_fd_io__refgen).

The IP also includes;

- Power, Ground cells (PG pads),

- Reset cells (XRES),

- Test pads,

- Analog pads,

- power detector,

- overlay cells.

The IP also includes all the relevant ESD clamps, diodes and trigger circuits to complete the I/O ring.

The I/O buffers can be configured as an input buffer, output buffer, or an I/O buffer.

The sky130_fd_io__gpio buffer includes a single-ended input buffer that can be configured for LVTTL, CMOS/I2C operation.

sky130_fd_io__gpiov2 has better electrical performance and the Rx can handle 1.8V signaling when the I/O supply is different from 1.8V.

sky130_fd_io__gpio_ovtv2 is fully I2C compliant and includes the over-voltage tolerance feature. It also has an input buffer that can support selectable trip-point feature along with a reference generator.

The sky130_fd_io__sio buffer can be configured to produce a regulated high output level, and includes a differential input buffer. All I/O buffers support multiple drive modes.

The IP supports a power supply range of 1.71V to 5.5V.

Features. Benefits, Tradeoffs, Limitations

- 1.71V-5.5V continuous supply operating range

- Rail-based ESD protection for sky130_fd_io__gpio* and sky130_fd_io__sio_macro

- I2C compliant sky130_fd_io__gpio_ovtv2

- I2C compatible - sky130_fd_io__gpiov2, sky130_fd_io__gpio, sky130_fd_io__sio

- CMOS, LPC compliant - sky130_fd_io__gpio*, sky130_fd_io__sio

- Low Power modes: Hibernate mode (Latch previous state), Deep Sleep Mode (allows I2C communication), Stop Mode (retains I/O state when LV supply is gone)

- Selectable output buffer drive modes (open drain high/low, strong/weak pull up/down, High-Z output) - sky130_fd_io__gpio*, sky130_fd_io__sio

- Regulated output high level - sky130_fd_io__sio

- Hot swap & over-voltage tolerant - sky130_fd_io__sio, sky130_fd_io__gpio_ovtv2

- Selectable output buffer slew rate control - sky130_fd_io__sio, sky130_fd_io__gpio*

- Selectable input buffer threshold (LVTTL or CMOS/I2C)- sky130_fd_io__gpio*, sky130_fd_io__sio

- Selectable 1.8V signaling (Active Mode) - sky130_fd_io__gpiov2, sky130_fd_io__gpio_ovtv2

- Selectable differential input buffer threshold (4 options) - sky130_fd_io__sio

- Integrated analog multiplexers (2) - sky130_fd_io__gpio*

- IP has multiple Power/Ground pads with HV and LV clamps, diodes, Test pads to enable I/O ring assembly

- VDDIO and VDDD power detector

- Multiple flavors of XRES cells

- For complete set of feature comparison, see Table 6.5

- AIP/LEDA rules set compliant : 5.0

Design Metrics

Table 6.1: Design Metrics-1

Description	Active Mode	Deep Sleep
Output: Fmax Freq	33MHz	33Mhz
Output: Fmax Freq	33MHz	33Mhz
SE Input: Fmax Freq	66MHz	66MHz
Number of power domains	5	
Number of power modes	- Active - Hibernate - Deep Sleep - Stop	
Single-ended Input buffer hysteresis (ALL I/O)	I2C complaint	
Rise/Fall trip point for VDDD detector	0.7V-1.5V	
Rise/Fall trip point for VDDIO detector	0.7V-1.5V	
Simulation Temperature Range	-40C to 100C	
- Simulation Voltage range I/O - Analog Supply	1.65V-5.5V	
- Simulation Voltage range I/O - LV Digital Supply	1.60V-1.95V	

Table 6.2: Design Metrics-2

sky130_fd_io__sio Differential Input buffer	2.0V	3.3V	5.0V
Quiescent current	0.23mA	0.25mA	0.27mA
ICC @ Fmax	0.35mA	0.40mA	0.50mA
Voltage trip point (SIO)	Vinref±200mV		

Table 6.3: Design Metrics-3

	`tt_leak` 3.0V, 25C	`leak` 3.0V, 85C
• sky130_fd_io__gpio* ISB • `enable_h` = 0	0.17nA	89.63nA
• sky130_fd_io__sio ISB • `enable_h` = 0	0.22nA	40.29nA

Table 6.4: Design Metrics-4

sky130_fd_io__gpio* AMUX switch resistance	• 275 : CSD Range • 1000 : Full Range

Configuration Options

- ALL I/O: Input and Output buffers can be enabled independently

- ALL I/O: Input buffer trip point select between CMOS/I2C & LVTTL

- ALL I/O: Configurable for 8 different Output drive modes

- ALL I/O: Output can be configured for different slew rates

- ALL I/O: I/O buffer can be configured into low power or low leakage mode using hold state control signals

- ALL I/O: O/P Buffer can be configured to drive the PAD during deep sleep mode

- sky130_fd_io__sio output buffer can be cured to be CMOS or Regulated output high level buffer (only in Strong Pull up mode)

- sky130_fd_io__gpiov2, sky130_fd_io__gpio_ovtv2 to handle 1.8V signaling on pad

- sky130_fd_io__gpio_ovtv2 input buffer supports selectable trip point feature

Typical Application

The SKY130 IO cells are typically used to build the I/O ring around the chip core. In addition to I/O's, Power/Ground cells, ESD clamps, Bond pad etc. are also available in this IP. I/O's are used to communicate with the external world and acts as the interface/buffer between the chip core and the external system.

Power Performance

The I/O's support multiple power modes (Hibernate, Deep Sleep, Stop) which are low-power modes, while still retaining the state of the I/O.

FMEA

Rail-Based ESD

The ESD strategy for M0S8 platform is non-distributed (grouped) rail-based ESD. This will be implemented across all pins and the ESD scheme can be fully simulated and easily portable across technologies.

Architecture and Implementation details

The different components needed to build the I/O ring are - sky130_fd_io__gpio sky130_fd_io__sio, ESD RC Clamps (which sit inside the Power/Ground PADS). Each external power domain will be protected with its own ESD RC clamp. There will be ESD diodes from each of the derived supplies to the source supply. For this purpose, two types of ESD RC clamps will be developed - HV Clamp and LV clamp.

Alternate XRES implementation

Todo: Only   sky130_fd_io__top_xres4v2   is   currently   available.   sky130_fd_io__top_xres_2   and sky130_fd_io__top_axresv2 are not yet available.

The glitch filter and 5k pull-up resistor in the current sky130_fd_io__top_xres_2 are provided as separate cells. A PMOS switch is used to disable the pull-up resistor.
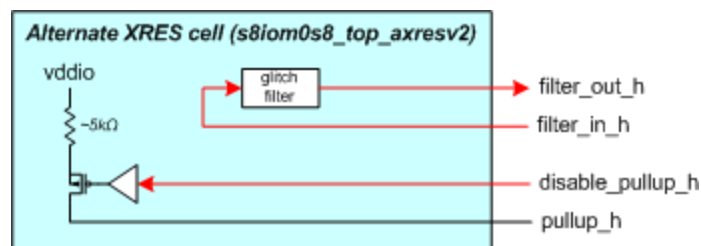
Fig. 6.1: Alternate XRES Implementation

Critical Requirements Summary

Overview of Block Applications

The Data I/O circuitry is used to communicate with other components in a PC board environment. The circuit also has the capability of shifting between core level voltages and I/O level voltages.

The buffers support a power supply range of 1.71V to 5.5V.

Block Architecture Overview

The following sections describe each of the blocks in detail:

- *Block Description*
- *I/O Common Features*
- *sky130_fd_io__gpio Additional Features*
- *sky130_fd_io__gpiov2 Additional Features*
- *sky130_fd_io__gpio_ovtv2 Additional Features*
- *sky130_fd_io__sio Additional Features*
- *sky130_fd_io__refgen (Reference Generator) Features*
- *sky130_fd_io__gpio_vrefv2 (Reference generator for Selectable trip point input buffer) Features*
- *:sky130_fd_io__top_vrefcapv2 Features*
- *sky130_fd_io__top_amuxsplitv2 Features*
- *PG pads (ESD)*
- *ESD design details*
- *XRES*
- *Test Pads (TP1, TP2, TP3)*
- *Overlay Cells*
- *Power detector*
- *sky130_fd_io Pin Information*
- *Timing Requirements and Diagrams*
- *Block Level Interfaces*
- *Reset and Initialization*
- *Power Modes*
- *Register Definitions*
- *Power Architecture and Modes*
- *Grounded Power Supplies*
- *Block behavioral model requirements*

Block Description

Todo: sky130_fd_io__gpio is not yet publicly available.

The SKY130 IO cells is a toolkit IP. It contains all the cells and primitives required to construct an I/O ring in the SKY130 technology.

Additional details of the cells included can be found in the sections below.

This sky130_fd_io library contained in this document covers different kinds of I/O cells, a general purpose I/O (sky130_fd_io__gpio) and a special I/O (sky130_fd_io__sio), a reference generator (sky130_fd_io__refgen) for providing voltage references to the sky130_fd_io__sio and Power and Ground (PG) cells that make up the I/O ring.

A single table comparison of all features across different IO's is provided in Table 6.5.

I/O[Page 245, 1] **Common Features**

Todo: Only sky130_fd_io__gpiov2 and sky130_fd_io__gpio_ovtv2 are currently available. sky130_fd_io__gpio and sky130_fd_io__gpiosf are not yet publicly available.

The sky130_fd_io__gpio and sky130_fd_io__sio buffers contain the following common features:

- *Eight drive strength modes*
- *Independent control of input and output buffer enables*
- *Input buffer threshold select*
- *I/O supply and Internal supply level input buffer outputs*
- *Selectable output edge rate control*
- *Hold state mode (latch previous state)*
- *I/O Mode Control Override during Power-up*
- *Pad Access to the Core*
- *O/P configuration to drive the PAD in hold mode*

The features that are supported by different I/O's are documented in Table 6.5 below:

---
[1] I/O (sky130_fd_io__gpio, sky130_fd_io__gpiosf, sky130_fd_io__gpiov2, sky130_fd_io__gpio_ovtv2, SIO).

Table 6.5: Comparison of features across different I/O's provided in this
IP

Feature	sky130_fd_io__gpio	sky130_fd_io__sio_	sky130_fd_io__gpio	sky130_fd_io__gpio_ovtv2
Drive Capability (Source)[2]	4mA	4mA	4mA	4mA
Drive Capability (Sink)	4mA[3]	20mA[5]	4mA[Page 246, 3]	10mA[3]
Drive Modes	8-Modes	8-Modes	8-Modes	8-Modes
Slew Rate Control	Slow/Fast	Slow/Fast	Slow/Fast	Slow/Fast/I2C
Input Buffer trip point	CMOS/TTL	CMOS/TTL	CMOS/TTL/1.8V	CMOS/TTL/1.8V/Selectable
Over-Voltage Tolerance	No	Yes	No	Yes
Analog Mux	2	0[4]	2	2
Regulated Output	No	Yes	No	No
Input buffer type	SE	SE+Diff	SE	SE
I2C Compliance	Limited[5]	Limited[5]	Standard,Fast	- Standard - Fast - Fast-Plus[6] - High-Speed
Low-voltage DFT support	No	No	Yes	Yes
Hysteresis[7]	5%	5%	10%[8]	10%[8]

Eight drive strength modes

The IP includes three static drive mode bits (dm<2:0>). These bits are used to configure the output buffer drive strength.
A default setting for enabling or disabling the input and output buffer is also defined. The eight drive strength modes
are defined in the following table.

---

[2] For 3V range. sky130_fd_io__sio configured in unregulated mode.

[3] VDDIO1.71V.

[5] Limited - Compliant for limited ranges of Vext, Rext and Cbus.

[4] SIO interacts with the analog mux for ADFT of sky130_fd_io__refgen.

[6] 20mA support for VDDIO>2.9V.

[7] Input Buffer operating at 48 MHz w hen VCCHIB=1.4V, VDDIO=1.65V

[8] For CMOS mode only.

Table 6.6: Truth table for I/O Drive Strength Modes

inp_dis	oe_n	dm<2:0>	Pad State out=1	out=0	Input Buffer	Output Buffer	Mode Description
X	X	000	Hi- Z	Hi- Z	Disabled (in=0)	Disabled	• Input/Output buffers disabled • Analog Input Mode
0	X	001	Hi- Z	Hi- Z	Enabled	Disabled	Configured as Input only
0	0	010	Res 1 (5k)	Strong 0	Enabled (in=0)	Enabled	• Weak pull-up, • strong pull-down
0	0	011	Strong 1	Res 0 (5k)	Enabled (in=0)	Enabled	• Strong pull-up • Weak pull-down
0	0	100	Hi- Z	Strong 0	Enabled (in=0)	Enabled	• Open Drain • Strong pull-down
0	0	101	Strong 1	Hi- Z	Enabled (in=0)	Enabled	• Open Drain • Strong pull-up
0	0	110	Strong 1	Strong 0	Enabled (in=0)	Enabled	• Strong pull-up • Strong pull-down

X = don't care 0/1

Independent control of input and output buffer enables

The I/O cells also include separate input disable `inp_dis` and output enable `oe_n` control signals as shown in Table 6.6. When `inp_dis` = 0 the input buffer is enabled and when `oe_n` = 0 the output buffer is enabled. When these signals are high (logic 1) the corresponding buffers are disabled independent of the state of the drive mode bits dm<2:0>. For example, if drive mode 2 (dm<2:0>=010) is selected, the input buffer is enabled by default. If `inp_dis`=1 for this drive mode, the input buffer enable default state will be overridden and the input buffer will be disabled and the input buffer output will be driven low.

Input buffer threshold select

The `vtrip_sel` signal alters the input buffer Vil and Vih specifications. The Vil and Vih specifications are listed in the following table.

Table 6.7: I/O Vil & Vih Specifications

Prameter	Description	Units	Condition	vtrip_sel=0	vtrip_sel=1
VIL	Input Low Voltage	V	• vddio < 2.7V • vddio > 2.7V	0.3 * vddio	• 0.3 * vddio • 0.8
VIH	Input High Voltage	V	• vddio < 2.7V • vddio > 2.7V	0.7 * vddio	• 0.7 * vddio • 2.0

When `vtrip_sel` = 0, the input buffer functions as a CMOS input buffer. When `vtrip_sel` = 1, the input buffer functions as an LVTTL input buffer.

I/O supply and Internal supply level input buffer outputs

The input buffer produces two outputs, a low voltage output and a high voltage output. The low voltage output is produced by level shifting the external `vddio` referenced level input to the internal `vcchib` level output. The high voltage output is produced by not level shifting the external `vddio` referenced level input to a buffered internal `vddio_q` level output.

Selectable output edge rate control

The CMOS output buffer includes a slew rate control input signal `slow`. When this signal is activated (slow = 1) the output edge rate will be slower than the default setting (slow = 0).

Hold state mode (latch previous state)

The I/O cell includes a hold state control signal `hld_h_n`. The purpose of this signal is to place the I/O cell into a low leakage mode while holding the previous state of the input controls, output controls and data. `hld_h_n` latches all control signals except `enable_h`. Specific timing constraints between the `hld_h_n` input and the other control signals must be satisfied to when entering and exiting the hold state mode. The Input signals which are latched by `hld_h_n` are dm<2:0>, slow, `vtrip_sel`, `inp_dis`, out, `oe_n`. The input signals, `ibuf_sel`, `vreg_en`, in sky130_fd_io__sio cell are also latched by `hld_h_n`.

During the hold mode, vccd can either be taken down to 0 or can float. During this case, the I/O input buffer would continue to actively drive out as long as there are valid power supplies (vddio, vddio_q and vcchib).

During the hold mode, the O/P can be configured to drive the PAD as described in Feature 9.

I/O Mode Control Override during Power-up

Todo: Only sky130_fd_io__gpiov2 and sky130_fd_io__gpio_ovtv2 are currently available. sky130_fd_io__gpio is not yet publicly available.

The sky130_fd_io__gpio includes an I/O mode control override signal `enable_h` that is different from the `oe_n` signal. The signal `enable_h=0` forces the output drive mode to Hi-Z. The `enable_h` signal is intended to be at logic 0 during the chip power-up sequence. During the power-up sequence this signal is driven low and the output driver is forced to a known state (Hi-Z). This ensures that the output driver does not enter a crow-bar condition.

Before the power-up sequence is completed, and the `enable_h` signal is asserted (logic 1), the data inputs and the control signals must be stable to ensure that the output driver does not inadvertently enter a crow-bar condition while exiting the power-up sequence.

The `enable_h` signal takes priority over the `hld_h_n` signal. In other words, when the I/O mode control override signal `enable_h` is logic 0 and the `hld_h_n` control signal is active, the output driver will be forced to drive Hi-Z. The previous states on the pull-up and pull-down signals will be over written and set to the levels required to force the driver. If the `hld_h_n` signal remains active after the `enable_h` signal transitions from logic 0 to logic 1, the forced condition (Hi-Z) will be held. Table 6.8 describes the `enable_h`, `hld_h_n` functionality.

Table 6.8: sky130_fd_io__gpio Mode Control Override & Hold State
Operation

enable_h	hld_h_n	Previous pad Output state	Current pad Output State	Notes
1	0	0	0	
1	0	1	1	
1	0	Hi-Z	Hi-Z	
1	1	Table 4.2-1	Table 4.2-1	
0	X	X	Hi-Z	• Input buffer disabled; • Output buffer Hi-Z (configured as dm<2:0>=000)

Note that there is no latch present on the `pad` itself, but the data `in` gets latched whenever `hld_h_n=0`. Further whenever `enable_h=0`, this data level shifter gets forced to a value which determines the `pad` current output state.

Pad Access to the Core

The I/O provides pad access to the core. `pad_no_esd_h` is directly connected to the pad. `pad_a_esd_0_h` and `pad_a_esd_1_h` is connected to the pad through a 150 ohm ESD resistor.

O/P configuration to drive the PAD in hold mode

The hold over ride signal (`hld_ovr`, active high, vcchib domain) signals the O/P buffer when to provide the flow-through functionality of the data input to the output buffer and output enable in deep sleep mode.

The functionality is defined in Table 6.9.

Table 6.9: Functionality during normal and hold modes

hld_ovr	hld_h_n	in	oe_n
0	0	Latched	Latched
0	1	Normal	Normal
1	0	Over-ride	Over-ride
1	1	Normal	Normal

Note:

- Latched means that the input and output enable are latched. This is the same functionality as mentioned in Table 6.7.

- Normal refers any mode other than Sleep modes

sky130_fd_io__gpio Additional Features

Todo: sky130_fd_io__gpio is not yet publicly available.

The block diagram for the sky130_fd_io__gpio is shown in Fig. 6.2. Note: Bus notation dm[3] denotes a 3 bit bus dm[2:0]. These notations are interchangeably used in the document.

All sky130_fd_io__gpio provides additional functionality of analog connectivity to the PAD for CSD and other applications as described below:

sky130_fd_io__gpio Analog Connectivity Modes

Todo: sky130_fd_io__gpio is not yet publicly available.

The M0S8 sky130_fd_io__gpio integrates the AMUXBUS switches to two `AMUXBUS_A` and `AMUXBUS_B` analog buses. These buses are used for both Capsense operation (as described in the CSD chapter), and general analog connectivity for Programmable Analog blocks and ADFT.

The analog functionality is controlled using three control signals.

- `analog_en` enables the analog functions of the sky130_fd_io__gpio cell

- `analog_sel` selects between `AMUXBUS_A` and `AMUXBUS_B`

- `analog_pol` selects the function of the `out` input, which toggles between AMUXBUS and VSSIO or between VDDIO and AMUXBUS

Table 6.10 describes the analog functionality as selected by the relevant control signals:

Table 6.10: Analog functionality by the relevant control signals

analog_en	analog_sel	analog_pol	Analog Function out=0	out=1	Digital Function Input	Output
0	X	X	N/C	N/C	Unaffected	Unaffected
1	0	0	Vssio	amuxbus_a	Disabled	Unaffected
1	0	1	amuxbus_a	Vddio	Disabled	Unaffected
1	1	0	Vssio	amuxbus_b	Disabled	Unaffected
1	1	1	amuxbus_b	Vddio	Disabled	Unaffected

Note that digital output driver can be used concurrent with analog function

Note the following: When the I/O is in an `analog` mode, the digital input buffer is disabled, but the output driver is not. Both CSD and certain Programmable Analog applications make use of the digital output driver as a driver on analog signals/nodes. The output driver performs the function as selected by its dm[3] inputs (which may be either OFF or not).

Note that these modes only concern analog functions `internal` to the sky130_fd_io__gpio, i.e. using the internal AMUXBUS switches.

Shielding for Analog Mux busses: AMUX switches can also be used to source and sink currents from CSD IDAC block to sky130_fd_io__gpio pins. The current IDAC for CSD block can be used to supply/ source current through AMUX to any sky130_fd_io__gpio pin. The maximum current can be up to 1mA and thus the AMUX layout needs to be designed keeping EM/IR considerations in mind.
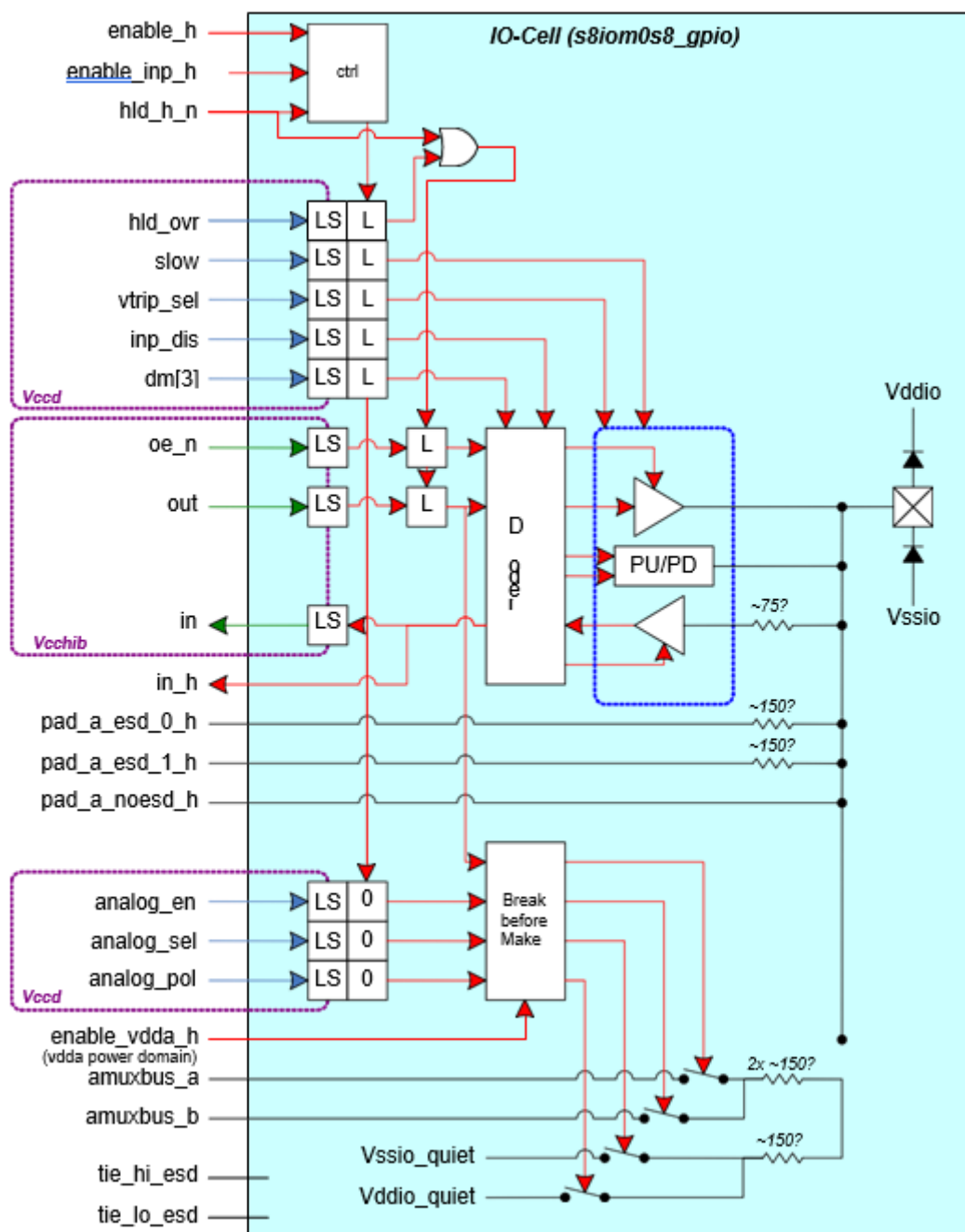
Fig. 6.2: Block diagram for sky130_fd_io__top_gpio

Usage of ``VSSIO_Q``in AMUX: The CSD pull-down transistor used in AMUX is the only one that uses the `vssio_q` connection to the I/O. In case the AMUX is used for CSD operation, `vssio_q` can alternatively be connected to VSSA without concerns for noise. Care must be taken that VSSIO and `VSSIO_Q` should not be shorted at VSSIO pad when used in this configuration.

Changes to Analog Mux for sky130_fd_io__gpiov2 and sky130_fd_io__gpio_ovtv2

Todo: sky130_fd_io__gpio is not yet publicly available.

1. The input buffer is no longer disabled inside sky130_fd_io__gpiov2 and sky130_fd_io__gpio_ovtv2 automatically when analog mux is enabled (`analog_en`=1). This was done to unblock self-testing of I/O cells. The firmware needs to ensure that `inp_dis`=1 when `analog_en`=1.

2. Power mode behavior was modified for both sky130_fd_io__gpiov2 and sky130_fd_io__gpio_ovtv2. An extra control signal `enable_vswitch_h` is added to have better control over the power mode behavior. The following table gives the supplies, control signals and their role:

Table 6.11: Supplies, control signals and their definition

Signal	I/O-Behavior
vddio	Digital supply for the I/O-cell. This supply is used to implement all digital input/output functions. It can be connected to the main system digital supply (vddd) or to an independent vddio supply.
vdda	Analog supply for the I/O-cell. This supply is used to implement the analog switches associated with amuxbus and CSD behavior. This supply is either connected to the global analog supply in the system or tied off to vddio when amuxbus functionality is not used.
vccd	The main regulated (1.8V) core supply. This supply is the relative supply of most of the configuration/control signals coming into the I/O-cell and is used for level translation only. No I/O circuits are powered using this supply.
vcchib	The hibernate regulated supply (1.8V). This supply is the relative supply for the I/O data interface (in, out, `oe_n`) and is also used mainly for level translation only. This supply can also be used as a reference for the sky130_fd_io__gpio input buffer.
enable_h	The master enable signal to the I/O-cell's digital section. This signal is in the vddio voltage domain. This signal is guaranteed to establish early during the vddio power ramp to enable glitch free operation during power up and down ramps. When asserted (1), this signal guarantees that vddio is valid and that either `hld_h_n=0` or all LV control signals are valid.
enable_i	This signal must be tied off to 0 or 1. Its value controls the power state of the input buffer when `enable_h=0`. This is a special feature used on 2 I/O-cells to allow for test-mode entry while XRES=0.
enable_v	The master enable signal to the I/O-cell's analog section. This signal is guaranteed to establish early during the power ramp to enable glitch free operation during power up and down ramps. It is used to power up/down all vdda powered circuits in the I/O-cell. When asserted (1), this signal guarantees that vdda and vddio are valid, and that either `hld_h_n=0` or all LV control signals are valid.
enable_v	A signal that controls the use of the pumped-up vswitch supply. When asserted (1), this signal guarantees that vswitch and vdda and vddio are valid, and that either `hld_h_n=0` or all LV control signals are valid.
enable_v	A signal that controls the use of the vcchib supply in some of the I/O circuits. When asserted (1), this signal guarantees that vcchib and all HV supplies are valid, and that either `hld_h_n=0` or all LV control signals are valid.
hld_h_n	This signal controls the iso-latches in the I/O-cell. It transitions low to freeze the state of the I/O-cell such that the active supply can be removed and the IO continues to function as configured.
hld_ovr	When `hld_h_n=1` this signal is ignored, when `hld_h_n=0` all control signals including this signal are frozen. The frozen value of this signal determines if the `out` and `oe_n` are frozen or not. 0: the I/O latches all of its configuration and control inputs as well as out and `oe_n`. 1: only the configuration and control inputs are latched. The logic in IOSS makes sure that `hld_ovr=1` never occurs when the system goes into STOP mode (which removes vcchib).

The normal operational state of the analog mux is when all supplies are present and all qualifiers asserted. However, there are many transient and special states that occur during power sequencing and during low power modes.

Input buffer enable during reset (`enable_inp_h`)

The `enable_inp_h` input determines the power on/off state of the digital input buffer when the I/O is disabled; i.e. `enable_h` is `0`. This pin is intended to be tied off to 0 or 1 (using the `tie_hi_esd` and `tie_lo_esd` signals on the I/O cell), depending on the need to have the input buffer enabled while `enable_h=0`. The truth table for `enable_inp_h` is given below in Table 6.12:

Table 6.12: `enable_inp_h` truth table

enable_h	enable_inp_h	• Inp_dis • dm[3]	Input Buffer State
0	0	X	Disabled
0	1	X	Enabled
1	X	Valid	F(`inp_dis`, dm[3])

Use of `enable_inp_h` at chip level: `enable_inp_h` is a hard-tie to either `tie_hi_esd` or `tie_lo_esd` of the sky130_fd_io__gpio and should not be register controlled. The `enable_inp_h` functionality is used to implement the Power-On-Reset Bypass Mode in SRSSv2: while XRES is asserted, SRSSv2 listens for a magic key on the SWD interface. This requires that primary SWD interface sky130_fd_io__gpio cells have their input buffers enabled, while XRES is asserted (`enable_inp_h` is `tie_hi_esd`). All other sky130_fd_io__gpio cells have their input buffers disabled while XRES is asserted (`enable_inp_h` is `tie_lo_esd`).

sky130_fd_io__gpiov2 Additional Features

The block diagram for sky130_fd_io__gpiov2 is shown below in Fig. 6.3. Note: bus notation dm[3] denotes a 3 bit bus dm[2:0]. These notations are used interchangeably in the document.

sky130_fd_io__gpiov2 provides all functionality as the original sky130_fd_io__gpio does. In addition, it provides the following extra features:

- Improved hysteresis of 10% across the entire supply range in CMOS mode

- Improved hysteresis of 100mV in LVTTL mode

- Improvements to meet I2C fall time with a certain minimum bus cap. Support only for Standard and Fast I2C modes. Table 6.14 gives the different output buffer configurations.

- Supports 1.8V signaling on PAD independent of vddio.

    1. Full spec support for Vcchib 1.6

    2. Limited functional support down to Vcchib 1.4 (Deep-sleep mode). 15Mhz CMOS operation.

- Improvements to the analog mux to support multiple power modes.

- Low-voltage DFT support (Input buffer runs at lower supply voltage than spec'ed)

Following additional pins have been added to support some of the above features:

- `ib_mode_sel`: This signal is used select between VDDIO and VCCHIB based thresholds (0=VDDIO, 1=VCCHIB)

- `enable_vddio`: This qualifier lets the sky130_fd_io__gpio know that VDDIO is either present (1) or absent (0) in VCCHIB domain. Currently, a skew of 100ns is allowed between `enable_h` and `enable_vddio`

- `enable_vswitch_h`: These qualifiers let the sky130_fd_io__gpio know that VSWITCH is either present (1) or absent (0) in VSWITCH domain
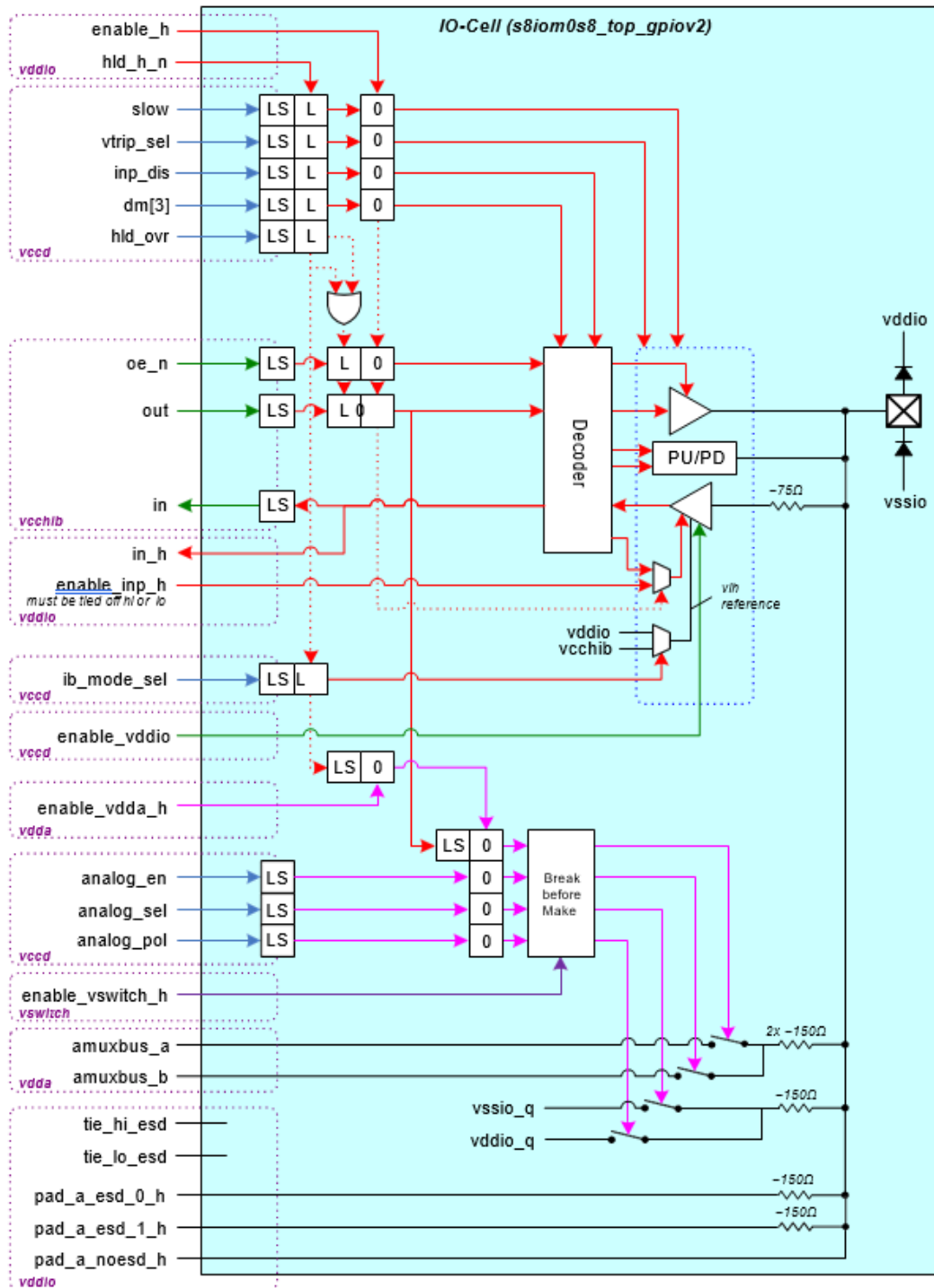
Fig. 6.3: sky130_fd_io__gpiov2 Block Diagram

Input Buffer selection for sky130_fd_io__gpiov2 is explained below in Table 6.13:

Table 6.13: Input Buffer Trip point selection for sky130_fd_io__gpiov2

Mode	`ib_mode_sel`	`vtrip_sel`	Input Buffer Trip Point	Description
CMOS	0	0	30%/70% of Vddio	CMOS input buffer
TTL	0	1	• VIL=0.8V, Vddio>2.7V • VIH=2.0V, Vddio>2.7V	LVTTL input buffer
VCCHIB	1	0/1	VIH=1.26V, VIL=0.54V	Supports 1.8V signaling on PAD

Note: If sky130_fd_io__gpiov2 or sky130_fd_io__gpio_ovtv2 is used to catch an external interrupt in hibernate mode, then care must be taken to have `ib_mode_sel` in logic 0 state before entering low-power modes.

This is because VCCHIB mode will not work in hibernate mode.

Table 6.14: sky130_fd_io__gpiov2 output buffer configurations

dm[3]	oe_n	slow	Driver PU (Rise Time Specs)	Driver PU (Rise Times- Sch)	Driver PD (Fall Time Specs)	Description
000/001	x	x	Disabled	Disabled	Disabled	Tri-state
x	1	x	Disabled	Disabled	Disabled	Tri-state
010	0	0	Resistive (5K)		Strong-Fast (2-12ns)	• WPU • SPD Mode • 25pF load
010	0	1	Resistive (5K)		Strong-Slow (10-60ns)	
011	0	0	Strong-Fast (2-12ns)		Resistive (5K)	• SPU • WPD Mode • 25pF load
011	0	1	Strong-Slow (10-60ns)		Resistive (5K)	
100	0	0	Open-Drain		Strong-Fast (2-12ns)	• OPD-PU • SPD Mode • I2C Standard Mode • I2C FS+ Mode
100	0	1	Open-Drain		I2C Fast Mode (6.22/20ns - 250ns)	• I2C Fast Mode • Cbus>200pF • Rext1K • Rext= tr/(0.8463*Cbus)
101	0	0	Strong-Fast (2-12ns)		Open-Drain	• SPU • OPD-PD Mode
101	0	1	Strong-Slow (10-60ns)		Open-Drain	• WPU • OPD-
110	0	0	Strong-Fast		Strong-Fast	• SPU

Mode

sky130_fd_io__gpio_ovtv2 Additional Features

sky130_fd_io__gpio_ovtv2 provides all functionality as sky130_fd_io__gpiov2 does. In addition, it provides the following extra features

- Over-voltage tolerant

- Provides better pull-down drive strength (V:sub:OL=0.6V @ I_{OL}=10mA for VDDIO=1.71V)

- Compliance to I2C standard, fast, fast-plus and high-speed modes

- Provides selectable trip points feature. Using an internal reference generator, input buffer trip points can be adjusted over a wide range of value. The max frequency of operation is 66MHz when input signaling is greater than 2.2V. When input signaling is between 1.8V and 2.2V, the max frequency is 33 MHz. The minimum value of input signaling for which full functional specs are met is 1.8v.

- sky130_fd_io__gpio_ovtv2 is not critical corner compliant as it uses the MIM cap from sky130_fd_pr library. sky130_fd_io__gpio_ovtv2 cannot be placed in corner of the die.

  Following additional pins have been added to support some of the above features:

- `ib_mode_sel<1:0>`: Used to configure input buffer trip points. Refer to Table 6.15

- `hys_trim`: Used to increase hysteresis feedback for input buffer in `Ref Mode`. Set to 1 for input signaling voltage > 2.2V and `0` otherwise.

- `slew_ctl<1:0>` : Used to vary slew rate in I2C mode (dm=100). Refer to Table 6.16

- `enable_vddio_lv`: This qualifier lets the sky130_fd_io__gpio know that VDDIO is either present (1) or absent (0) in VCCHIB domain

- `enable_vswitch_h`: This qualifier lets the sky130_fd_io__gpio know that VSWITCH is either present (1) or absent (0) in VSWITCH domain

Feature: Selectable Trip point feature

The input buffer in sky130_fd_io__gpio_ovtv2 supports the following modes as given in Table 6.15 below:
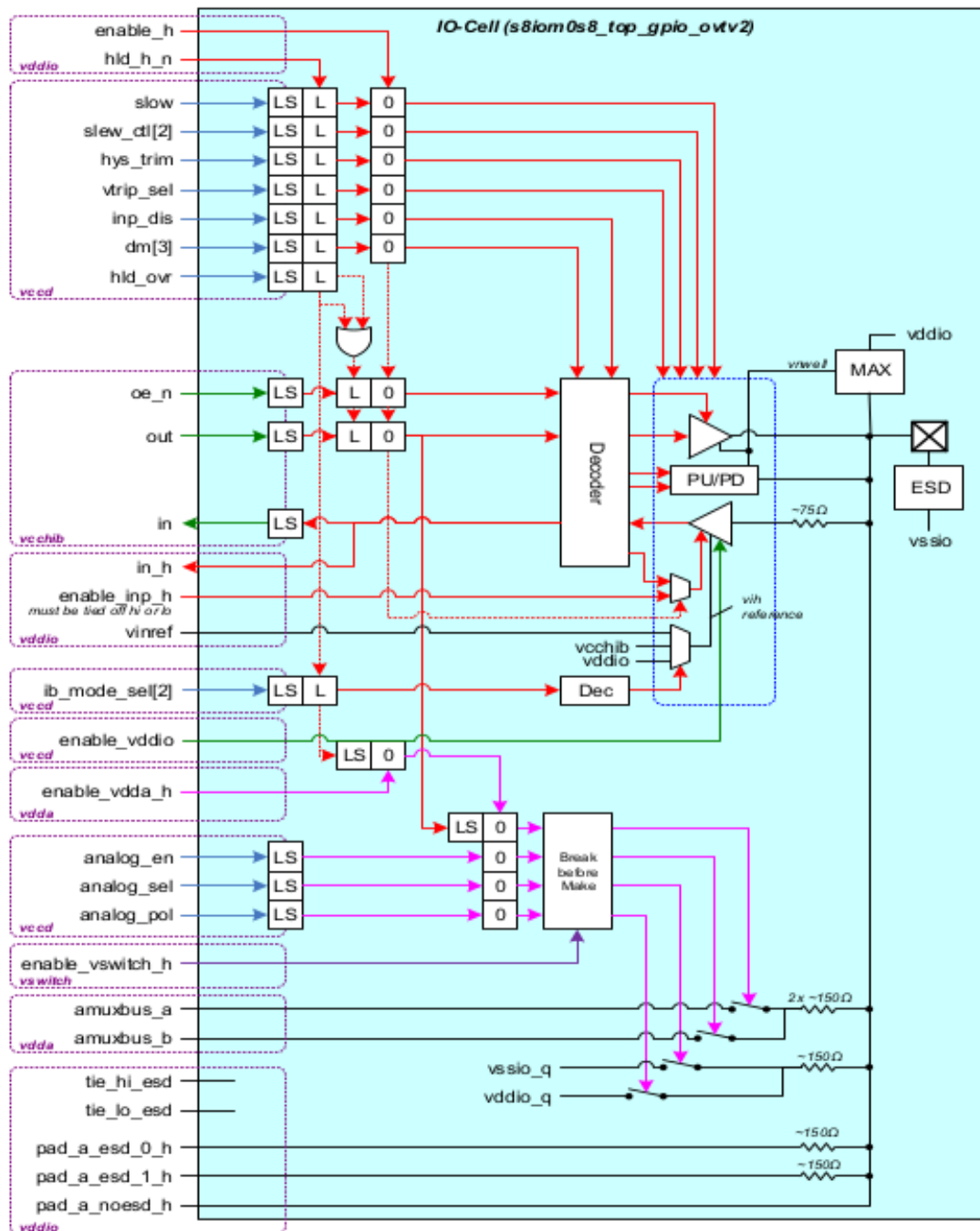
Fig. 6.4: sky130_fd_io__gpio_ovtv2 Block Diagram

Table 6.15: Input Buffer modes in sky130_fd_io__gpio_ovtv2 and their description

Mode	ib_mode_sel <1:0>	vtrip_sel	Input Buffer Trip Point	Description
CMOS	00	0	30%/70% of Vddio	CMOS input buffer
TTL	00	1	- VIL=0.8V - Vddio>2.7V - VIH=2.0V - Vddio>2.7V	LVTTL input buffer
VCCHIB	01	0/1	- VIH=1.26V - VIL=0.54V	Supports 1.8V signalling on PAD
Ref	10/11	0/1	30%/70% of `vinref`	- vinref = VDDIO*(13n+184)/600 - This feature works in conjunction with: :sky130_fd_io__top_gpiovref :sky130_fd_io__top_vrefcapv

Table 6.16: sky130_fd_io__gpio_ovtv2 Slew rate control with slow and slew_ctl<1:0>

dm[3]	oe_n	slow	slew_ctl[2]	Driver PU (Fall Time Specs)	Driver PD (Fall Time Specs)	Description
• 000 • 001	x	x	x	Disabled	Disabled	Tri-state
x	1	x	x	Disabled	Disabled	Tri-state
010	0	0	x	Resistive (5K)	Strong-Fast (2-12ns)	• WPU • SPD Mode • 25pF load • SPU • WPD Mode • 25pF load
010	0	1	x	Resistive (5K)	Strong-Slow (10-60ns)	
011	0	0	x	Strong-Fast (2-12ns)	Resistive (5K)	
011	0	1	x	Strong-Slow (10-60ns)	Resistive (5K)	
100	0	0	x	Open-Drain	Strong-Fast (2-12ns)	• OPD-PU • SPD Mode
100	0	1	11	Open-Drain	• HS mode (Vext=<2.8, F=1.7MHz) (10-80ns) • FS+ mode, Vext<=2.8V (20-120ns)	To be used in I2C mode
			01		• HS mode (Vext>2.8, F=1.7MHz) (10-80ns) • FS+ mode, Vext>2.8 (20-120ns)	
			10		HS mode (Vext<3.3) (20-160ns)	
			00		• HS mode (Vext>3.0) • FS mode	

sky130_fd_io__sio Additional Features

The block diagram for Special I/O (sky130_fd_io__sio) macro is shown below in Fig. 6.5
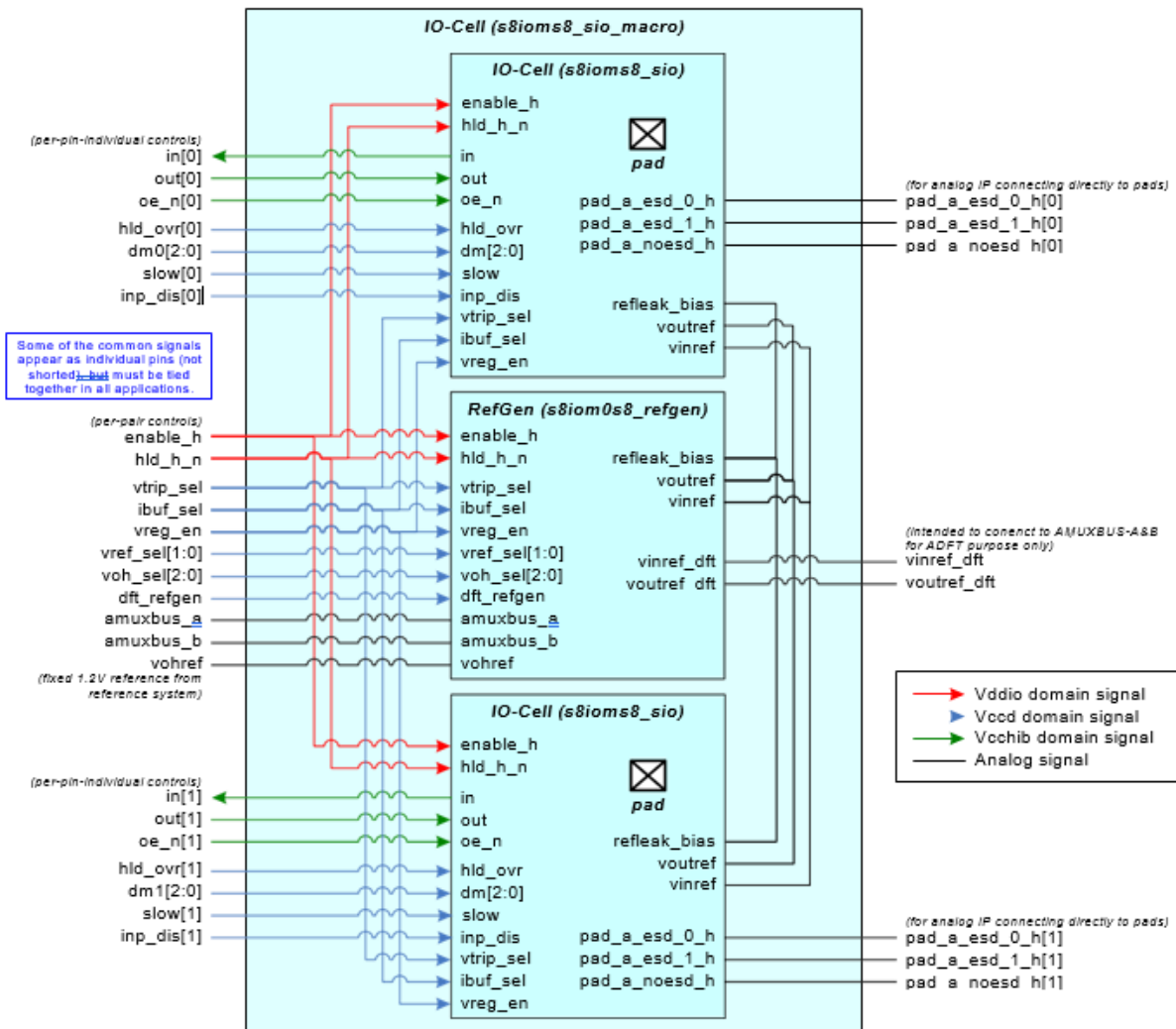
Fig. 6.5: Block diagram of sky130_fd_io__sio_macro

The sky130_fd_io__sio_macro consists of 2 sky130_fd_io__sio cells (Fig. 6.6) and a Reference generator cell. The sky130_fd_io__sio cells are ONLY available as pairs. The block diagram of sky130_fd_io__sio is shown below in Fig. 6.6. Note that dm[3] denotes a 3 bit bus dm[2:0]. These notations are used interchangeably in the document.

1. I/O-Cell sky130_fd_io__sio

The sky130_fd_io__sio provides the following additional features over the sky130_fd_io__gpio:

- Regulated output buffer

- Differential input buffer

The sky130_fd_io__sio cell adds a differential input buffer and a means for controlling or regulating the output buffer output high voltage level (Voh). The sky130_fd_io__sio cell has two additional control inputs (`vreg_en`, `ibuf_sel`), and an input buffer reference voltage (`vinref`), and an output buffer reference voltage (`voutref`). The added control inputs are used to select the input buffer type (single ended or differential) and output buffer type (CMOS or regulated).
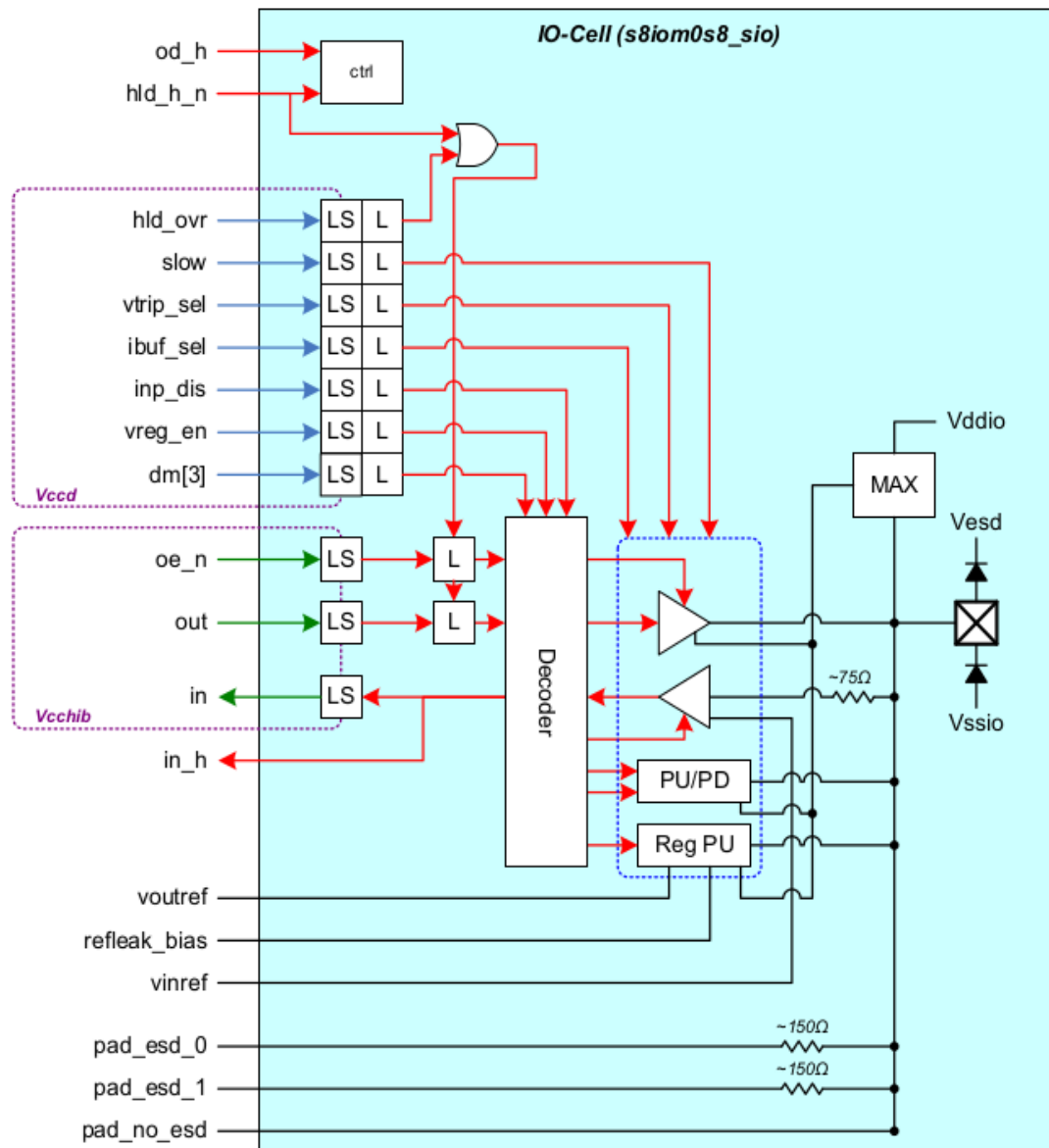
Fig. 6.6: Block diagram for sky130_fd_io__top_sio

The input buffer configuration is selected based on the state of the `ibuf_sel` control input. If this signal is low the standard single ended (sky130_fd_io__gpio) input buffer is selected, otherwise the differential input buffer is selected.

The following tables 13 and 14 describe the sky130_fd_io__sio cell configurations based on the added control signals.

Table 6.17: sky130_fd_io__sio Input Buffer Truth Table

ibuf_sel	Vref_sel [1:0]	voh_sel [2:0]	vtrip_sel	Trip Point (Vin-ref)	Description
0	X	X	0	30% / 70%	CMOS input buffer w/wo Hysteresis
0	X	X	1	• min (0.8V,30%) • min (2.0V,70%)	LVTTL input buffer w/wo Hysteresis
1	00	X	0	50% of vddio	Differential input buffer
1	00	X	1	40% of vddio	Differential input buffer
1	01	000	0	0.5 * Vohref	Differential input buffer
1	01	000	1	Vohref (buffered)	Differential input buffer
1	10/11	000	0	0.5 * amuxbus_a/b	Differential input buffer
1	10/11	000	1	amuxbus_a/b (buffered)	Differential input buffer

The `vreg_en` control input selects the output buffer configuration. If this signal is low the standard CMOS (sky130_fd_io__gpio) output configuration is selected. The regulated output configuration is selected ONLY if the dm<2:0> bits are correctly set to the strong pull up configuration. If the dm bits are set to any other configuration other than strong pull up, the regulated output buffer will be disabled, and the standard CMOS output buffer would take over.

Note: The `voh_sel[2:0]` combinations are found in the Table 6.20

Notice that the input buffer and output buffer configurations can be selected independently. For example, the standard single-ended input buffer and the regulated output buffer can be selected.

sky130_fd_io__refgen (Reference Generator) Features

The block diagram of sky130_fd_io__refgen used in sky130_fd_io__sio_macro is shown below in Fig. 6.7:

The sky130_fd_io__refgen block sky130_fd_io__top_refgen is an opamp connected in negative feedback loop configuration to generate the output reference voltage `voutref`. The input to the opamp (vref) can be selected from any of the three input references (vohref, `amuxbus_a` or `amuxbus_b`). The input reference is selected based on the control input `vref_sel[1:0]` (Table 6.6). The voltage voutref is `voh_out`+`Vgs` (diode-connected nFET). In the Regulated Output Buffer, the voltage voutref is applied to the gate of a nFET (of the same type as the diode-connected nFET used to generate the voutref signal) and the output is the source of that nFET.

Consequently, this configuration compensates for the V_{GS} voltage drop of the source follower in the Regulated Output Buffer circuit and allows its output to be pulled to the desired V_{OH} voltage level, nominally equal to vohref value. The actual V_{OH} level and its tolerance relative to the vohref voltage depends on the output current load conditions. The
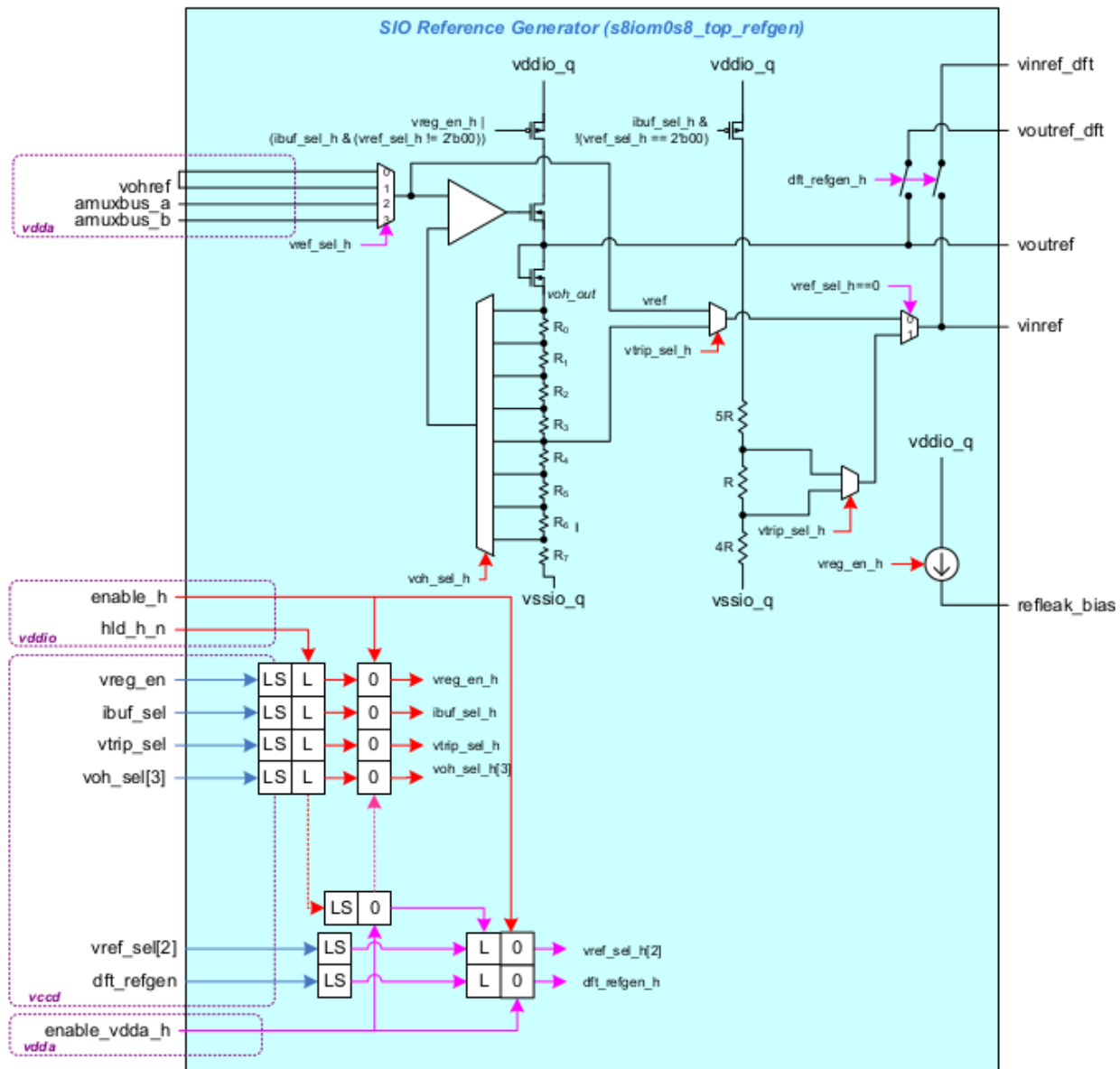
Fig. 6.7: Block diagram for sky130_fd_io__refgen

acceptable variation in V_{OH}-vohref tolerance versus output current load is specified in DC Specification tables. For a given input reference, vref, the value of voutref can varied by selecting different tap point from the resistive divider in the feedback path (Fig. 6.7). The resistors are not equal in value and are skewed to generate standard voltages (1.2, 1.5, 1.8, 2, 2.5, 3.3, 4.8), when the bandgap voltage (1.2V) is connected to vohref. This selection is based on the select signals , `voh_sel[2:0]` (Table 6.20). The output regulated value (`voh_out`) equals `vref/n`, where n=Rtap/Rtotal (Table 6.20).

Table 6.18: Input Reference selection

Vref_sel [1:0]	Ref.Selected
00	Vohref
01	Vohref
10	amuxbus_a
11	amuxbus_b

Note: The voltage range for the analog reference inputs (`vref/amuxbus_a/amuxbus_b`) is 1.0-4.6V and is dependent on the I/O supply, shown in Table 6.19 below.

Table 6.19: Analog Reference Input

I/O Supply (vddio)	analog input to reference (`vref/amuxbus_a/amuxbus_b`)
1.65V <= vddio < = 3.7V	1 - (vddio-0.5)
3.7V< vddio <= 5.6V	1 - (vddio-1)

Table 6.20: V_{OH} reference selection

voh_sel[2:0]	n = Rtap/Rtotal
000	1
001	0.8
010	0.67
011	0.6
100	0.48
101	0.4
110	0.36
111	0.25

Note:

- All the `voh_sel[2:0]` values cannot be selected for entire reference range (1V-4.6V). The upper value on VOH is limited to `Vddio_q - 400mV`.

- The resistors are not equal in value and are skewed to generates standard voltages (1.2, 1.5, 1.8, 2, 2.5, 3.3, 4.8), when band-gap voltage (1.2V) is connected to vref.

The input buffer reference `vinref` can be derived from four sources: vinref, half of `voh_out`, and 40% or 50% of the I/O supply voltage `vcc_io`. The `vinref` voltage level selected is based on the input buffer voltage trip point select `vtrip_sel` and voltage reference select `vref_sel` control inputs.

The truth tables for sky130_fd_io__refgen are shown in Table 6.21 and Table 6.22.

Important notes about sky130_fd_io__sio macro:

- Each pair of sky130_fd_io__sio's share a single RefGen block. This block allows for the generation of a `regulated mode` selectable input buffer trip point and output driver level.

- The I/Os retain the ability to disable the input buffer for I/O's with an active analog function. For sky130_fd_io__sio's not connected to any analog component this input must be tied off.

- The input reference (Vohref) to the RefGen block is assumed to be 1.2V.

- The RefGen block also connects to `amuxbus_a` and `amuxbus_b` for reference generation. Use case: An external pin as reference voltage.

- Regulated output buffer mode and differential input buffer mode cannot be used in low-power modes where VCCD is unavailable. It is the responsibility of firmware to ensure that the sky130_fd_io__sio is not configured in these modes before entering low-power modes.

- If sky130_fd_io__sio_macro is being used as an I2C pin to drive SDA, the following configuration bits need to be set (CMOS input buffer and open-drain output)—The configuration bits are given w.r.t a single sky130_fd_io__sio

    - dm<2:0>=100 (To enable the 20mA driver (I2C FS+ mode and input buffer)

    - `ibuf_sel=0` (To enable the SE buffer)

    - `inp_dis=0` (To enable input buffer)

    - `vtrip_sel=0` (To enable CMOS input buffer mode)

- All other control signals are don't care. The refgen can be disabled when sky130_fd_io__sio_macro is used for I2C (`vreg_en_refgen=0`)

Table 6.21: Valid sky130_fd_io__sio Differential Input Buffer Reference Voltage

Vref_sel <1:0>	vtrip_sel	Vinref
00	0	0.5 * `vcc_io`
00	1	0.4 * `vcc_io`
01	0	0.5 * `voh_out`
01	1	vref
10	0	0.5 * `voh_out`
10	1	vref
11	0	0.5 * `voh_out`
11	1	vref

Table 6.22: sky130_fd_io__refgen Truth Table

vohref	vreg_en	ibuf_sel	vref_sel <1:0>	voutref	vinref
X	0	0	X	Hi-Z	Hi-Z
1	0	1	00	Hi-Z	1
1	0	1	01,10,11	1	1
1	1	0	00,01	1	Hi-Z
X	1	0	XX	1	Hi-Z
1	1	1	00,01	1	1
X	1	1	10,11	1	1

Use of `dft_refgen` for ADFT purpose:

- The sky130_fd_io__refgen block produces two references to be used in the sky130_fd_io__sio_macro. `vinref` is the reference to the differential input buffer and `voutref` is the reference to the regulated output buffer.

- In order to have 100% ADFT coverage, these two references are bought out to the interface of the sky130_fd_io__sio_macro. By enabling `dft_refgen`, these two outputs of refgen can be observed on

`vinref_dft` and `voutref_dft`. In order to observe these two pins on any sky130_fd_io__gpio pins, these two pins need to be hooked to the analog busses and bought to any sky130_fd_io__gpio pad through the AMUXBUS inside the sky130_fd_io__gpio.

sky130_fd_io__gpio_vrefv2 (Reference generator for Selectable trip point input buffer) Features

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Todo: sky130_fd_io__gpio_vrefv2 is not yet publicly available.

This cell provides a reference (`vinref`) to the selectable trip point buffer in sky130_fd_io__gpio_ovtv2. This reference generator is a low-leakage resistive ladder whose tap points are selected based on the signaling required at the sky130_fd_io__gpio_ovtv2 pad. The block diagram is shown below in Fig. 6.8. Note ref_sel[5] denotes a 5 bit bus `ref_sel[4:0]`. These notations are used interchangeably in the document.
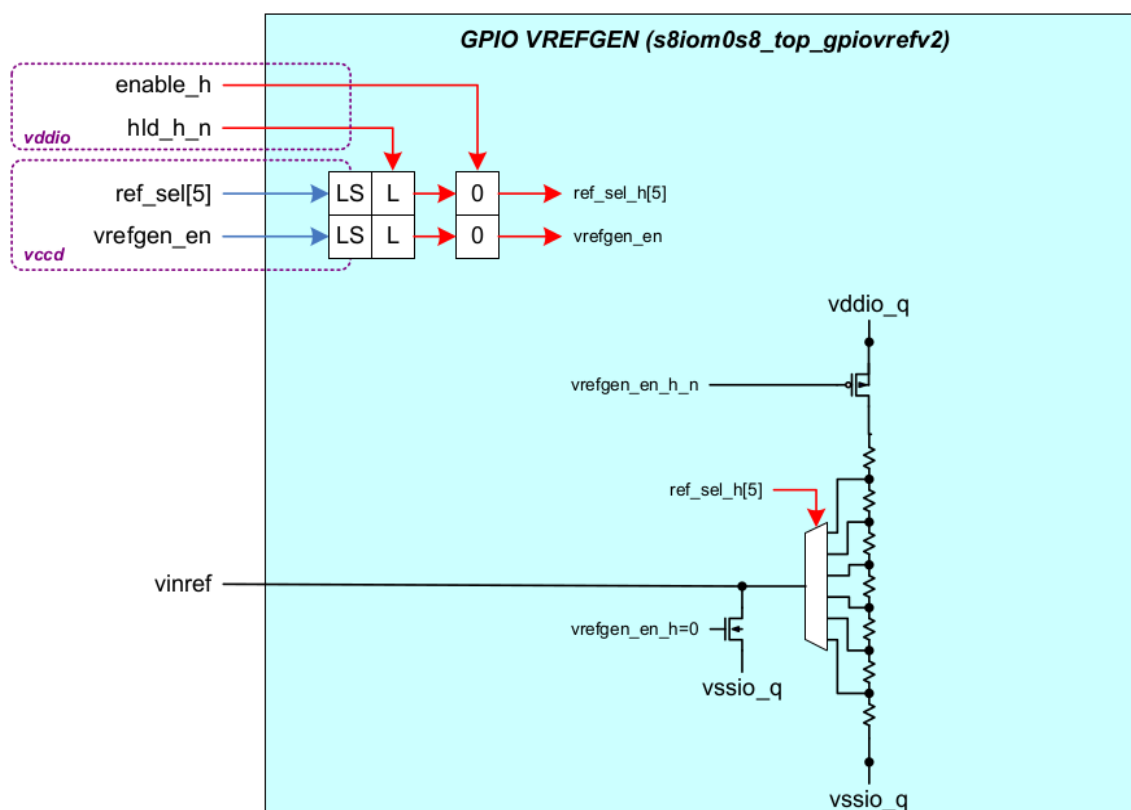
Fig. 6.8: sky130_fd_io__gpio_vrefv2 Block Diagram

The reference selection is based on the signaling range that needs to be at the PAD. For this to work, the external signaling range must be lower than VDDIO. The tap point selection is based on the formula:

vinref = (13n+184)*VDDIO/600

- Where vinref represents the input signaling voltage at sky130_fd_io__gpio_ovtv2 pad

- VDDIO is the supply voltage to the sky130_fd_io__gpio

- `n` is the tap point selection that gives us required vinref. Binary coding of `n` is `ref_sel<4:0>`. `n` should be chosen such that `vinref` is greater than 1.8V

For example:

- – Need to support 1.8V (vinref) signaling on PAD with VDDIO=5.0V. Plugging these numbers into the equation yields:

    1.8 = (13n+184)*5.0/600

    n= 2.46

- – As n=2.46, `ref_sel<4:0>` can be selected as either 2 (5'b00010) or 3 (5'b00011). This would give out a reference of `1.75V` and `1.858V` respectively.

- – Use a ceiling on `n` i.e. if n=2.46, use n=3 instead of n=2.

:sky130_fd_io__top_vrefcapv2 Features

Todo: sky130_fd_io__top_vrefcapv2 is not yet publicly available.

This cell contains a unit capacitance (4pF) that is intended to be placed on the `vinref` node that goes to multiple sky130_fd_io__gpio_ovtv2 cells. This is a filter cap used to suppress kick-back noise from the input buffers. The usage is shown below in Fig. 6.9:

sky130_fd_io__top_amuxsplitv2 Features

Todo: sky130_fd_io__top_amuxsplitv2 is not yet publicly available.

The amux splitter cell is designed to provide large chips (with large number of sky130_fd_io__gpio's) to break the analog mux into multiple segments. This cell is capable of grounding, disconnecting or feeding through each amuxbus. The block diagram is shown below in Fig. 6.10.

Each T-switch has 3 control signals coming to control the state of the switches. These are expected to be static switches. During power-up `(enable_vdda_h=0)` and low-power modes `(hld_vdda_h_n=0)`, the switches of the amux splitter are open.

General guidelines for the T-switch: Break before make logic that needs to be followed when working with the switch control signals. For example - when `amux_a_l` and `amux_a_r` are Independent, the mid-node of the switch needs to be closed to prevent unwanted coupling between the two amuxbus's. When connecting `amux_a_l` and `amux_a_r` care must be taken to disconnect the mid-node and then close the right and left switch.

PG pads (ESD)

Todo: sky130_fd_io__top_hvclamp_wopad, sky130_fd_io__top_hvclamp_wopadv2, sky130_fd_io__top_power_padonlyv2, and sky130_fd_io__top_ground_padonlyv2 are not yet publicly available.

The I/O library consists of Power (P) and Ground (G) pads that have RC ESD clamps embedded in them. There are two types of RC ESD clamps that are present in these PG pads.

- • HV clamp- Only one HV (High Voltage) clamp is present underneath the PG pads whose terminals can be connected independently without interfering with the PG connections
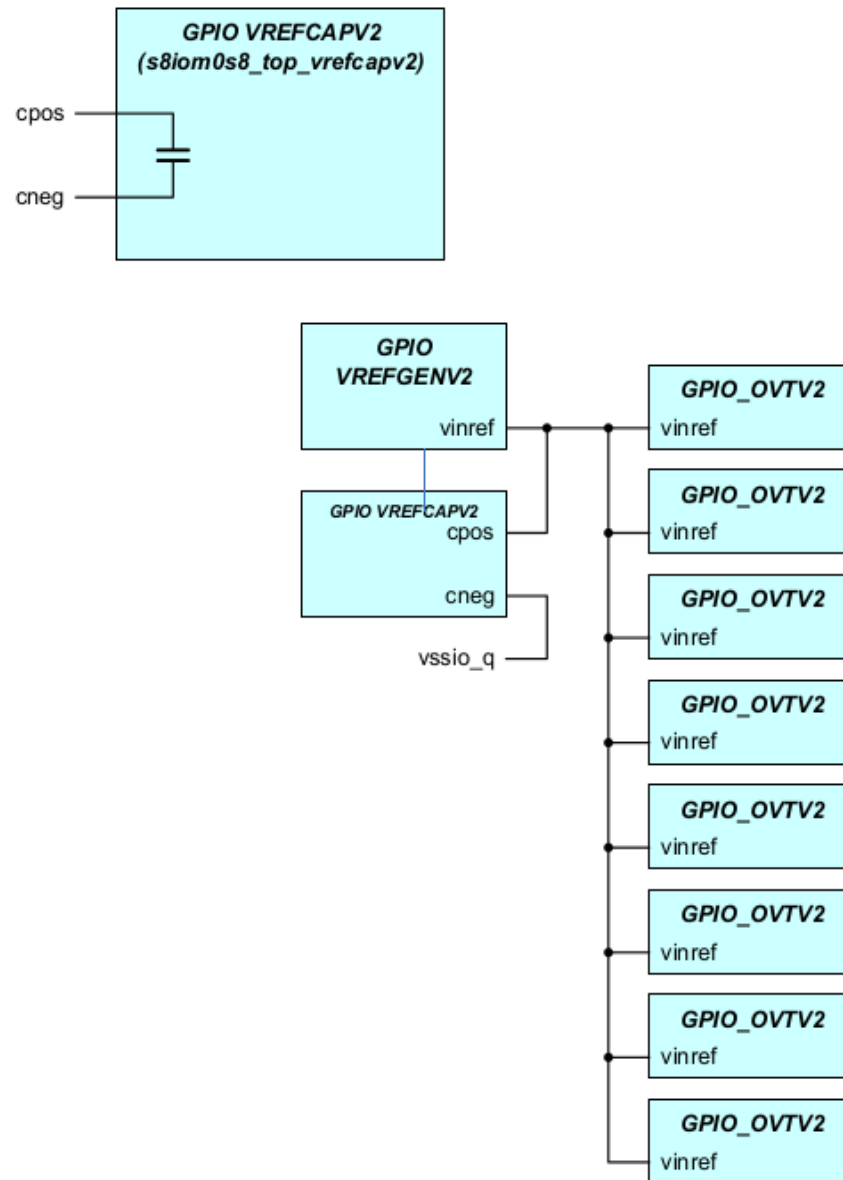
Fig. 6.9: sky130_fd_io__top_vrefcapv2
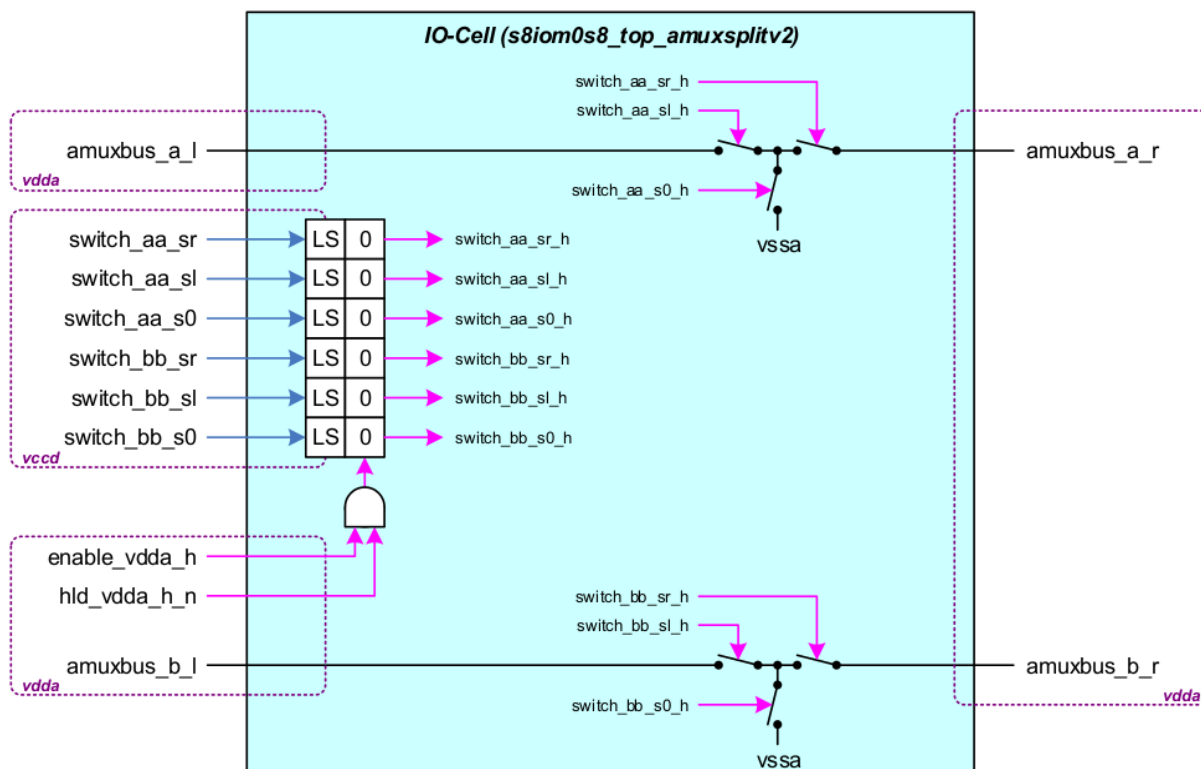
Fig. 6.10: Block diagram of sky130_fd_io__top_amuxsplitv2

- LV clamp- Two LV (Low Voltage) clamps and a B2B (back 2 back) diode can be accommodated underneath the PG pads. The two LV clamps have a total of six terminals that can be tied according to chip-level needs. The B2B however should be connected to the source/body of LV clamp1 and another independent ground node (bdy_b2b).

A layout variant of the HV clamp without pad is sky130_fd_io__top_hvclamp_wopadv2. This is a derivative of sky130_fd_io__top_hvclamp_wopad with following changes:

- Vssd pin added: P-substrate connection

- HV clamp gate connection improved.

- HV clamp source/drain connection improved.

Two additional pad cells to be used for power and ground connections added, namely:

- sky130_fd_io__top_power_padonlyv2

- sky130_fd_io__top_ground_padonlyv2

These are only M4/M5 pad structures with a short element. They are used to provide pad structure/connection to wopad clamps.

Integration Guidelines

Todo: Only sky130_fd_io__gpiov2 and sky130_fd_io__gpio_ovtv2 are currently available. sky130_fd_io__gpio is not yet publicly available.

All power and ground pads have the I/O bussing running through them in M5/M4, thereby forming an I/O ring when abutted to each other. The power and ground pads can be abutted to either the sky130_fd_io__gpio or the sky130_fd_io__sio_macro.

The Power and Ground pads are designed in such a way that one side of it is full DRC complaint to any sky130_fd_io__gpio or sky130_fd_io__sio_macro that abuts it. However due to limited area constraints, the other side cannot be abutted directly to a sky130_fd_io__gpio/sky130_fd_io__sio_macro. This puts a restriction that 2 pads (power/ground) should be paired to build the I/O ring.

ESD design details

Todo: sky130_fd_io__top_hvclamp_wopad_sio and sky130_fd_io__gpio are not yet publicly available.

The architecture for the RC ESD clamps trigger circuit is the simple one-time constant RC trigger circuit. For the over-voltage tolerant sky130_fd_io__sio, use ESD rail clamp sky130_fd_io__top_hvclamp_wopad_sio.

The HV and LV RC ESD clamps are robust up to 3.3KV HBM.

ESD HV RC ESD Clamp design

- Single trigger - 2us time constant
- Driver width of 2880 um was used
- Cell height the same as the sky130_fd_io__gpio

Usage of Outer Guard ring Connection (OGC) in ESD HV and LV clamps for sky130_fd_io

Todo: sky130_fd_io__top_hvclamp_wopad, sky130_fd_io__top_lvclamp_b2b_wopad, and sky130_fd_io__top_lvclamp are not yet publicly available.

Power and Ground pads in sky130_fd_io library come along with ESD HV and LV clamps embedded within them. All the ESD clamps are independent of the power or ground pads providing maximum flexibility, thereby making the end user make proper connections to the ESD clamps. The end user chip lead is the best-informed person about making these connections and must approve all the ESD connections.

One of the clamp connections is the outer guard ring connection (`ogc_hvc/ogc_lvc`). The basic purpose of this is to connect the outer guard ring (deep nwell) to provide noise isolation. The recommended usage of this is to connect it to a HV supply that is available all/most of the time.

Bottlenecks during implementation: The power and ground pads that contain the ESD clamps have a number of pins coming to the boundary interface. In order to minimize the resistance inside the cell to these ESD clamps, some of the `ogc_\*` connections are floated and connected internally to VDDIO.

The following Table 6.23 lists the different cells in sky130_fd_io library that have this `ogc_\*` connection and the recommended way to connect them.

Table 6.23: OGC connection and Usage

S.No	Public Cell	Internally connected?	Recommended connection to end user
1	sky130_fd_io__top_power_h	YES (VDDIO)	No need to connect
2	sky130_fd_io__top_ground_l	YES (VDDIO)	No need to connect
3	sky130_fd_io__top_power_lv	YES (VDDIO)	No need to connect
4	sky130_fd_io__top_ground_l	YES (VDDIO)	No need to connect
5	sky130_fd_io__top_hvclamp	NO	Connect to HV Supplythat is always present
6	sky130_fd_io__top_lvclamp_	NO	Connect to HV Supply that is always present (Outer guard ring is HV rules compliant)
7	sky130_fd_io__top_lvclamp	NO	Connect to HV Supply that is always present (Outer guard ring is HV rules compliant)

XRES

Todo: Only sky130_fd_io__top_xres4v2 is currently available. sky130_fd_io__top_xres, sky130_fd_io__top_xres_2, sky130_fd_io__top_xres2v2, sky130_fd_io__top_xres3v2, and sky130_fd_io__top_axresv2 are not yet available.

The XRES cell is a macro that is used to influence the internal system wide reset. The purpose of this cell is to provide a noise free signal from the input buffer to the core. Any glitch of 50ns or less on the XRES pad is rejected by the XRES macro.

The XRES cell (sky130_fd_io__top_xres, sky130_fd_io__top_xres_2) is a cell that integrates the input buffer from the sky130_fd_io__gpio and an HV RC filter. It also has a 5k weak pull up on the XRES pad.

The XRES cell has two outputs, out (LV) and `out_h` (HV). The HV output will be functional even when the LV supply to the input buffer is gone (STOP mode).

There are 5 variants of XRES cells in sky130_fd_io IP:

1. sky130_fd_io__top_xres and sky130_fd_io__top_xres_2

The two versions are the same except for layout differences.

2. sky130_fd_io__top_xres2v2

This cell is essentially a copy of the current sky130_fd_io__top_xres_2 cell. One minor layout modification is made to this cell which is to make the height of the new cell=200u (sky130_fd_io__top_xres_2 has 198u height). No change in functionality compared to current sky130_fd_io__top_xres_2.
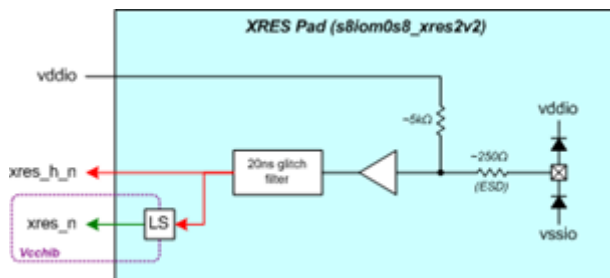
Fig. 6.11: sky130_fd_io__top_xres2v2

3. sky130_fd_io__top_xres3v2

This cell is also a copy of the sky130_fd_io__top_xres_2 cell but with the pull-up disabled. (I.e. pull-up metal connection will be cut).

There is a metal option provided to connect the pullup back on if required. This requires 2 extra pins in this cell.
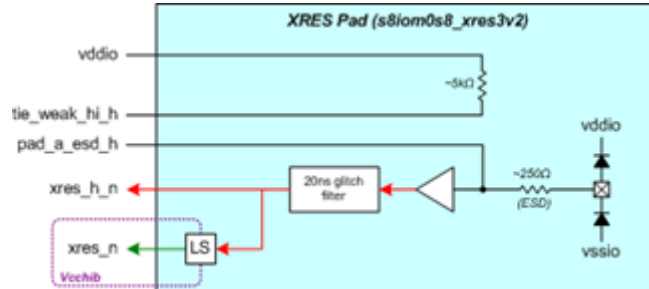
Fig. 6.12: sky130_fd_io__top_xres3v2

4. sky130_fd_io__top_axresv2

Glitch filter to filter out pulses less than 50ns pulse width. This glitch filter currently resides inside of the xres cells. In order to provide more flexibility, the glitch filter portion of the existing xres cell will be copied into this new public cell.

Pull-up cell to connect the pad to the power supply (vddio) through a 5k ohm resistor. A control bit (`disable_pullup_h`) is used to enable/disable the pull-up.
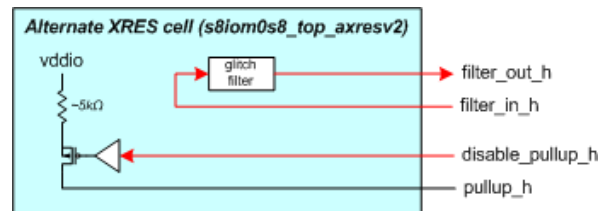
Fig. 6.13: sky130_fd_io__top_axresv2

Use case for the XRES cells

Usage guidelines on when to use the different cells:

sky130_fd_io__top_xres:

The first XRES cell sky130_fd_io__top_xres can ONLY be abutted to the sky130_fd_io__sio_macro on its right and to TP2 on its left. This will not have any physical verification errors with the above mentioned placement of sky130_fd_io__top_xres cell. This cell CANNOT be abutted with any other cells in the sky130_fd_io library to form the I/O ring.
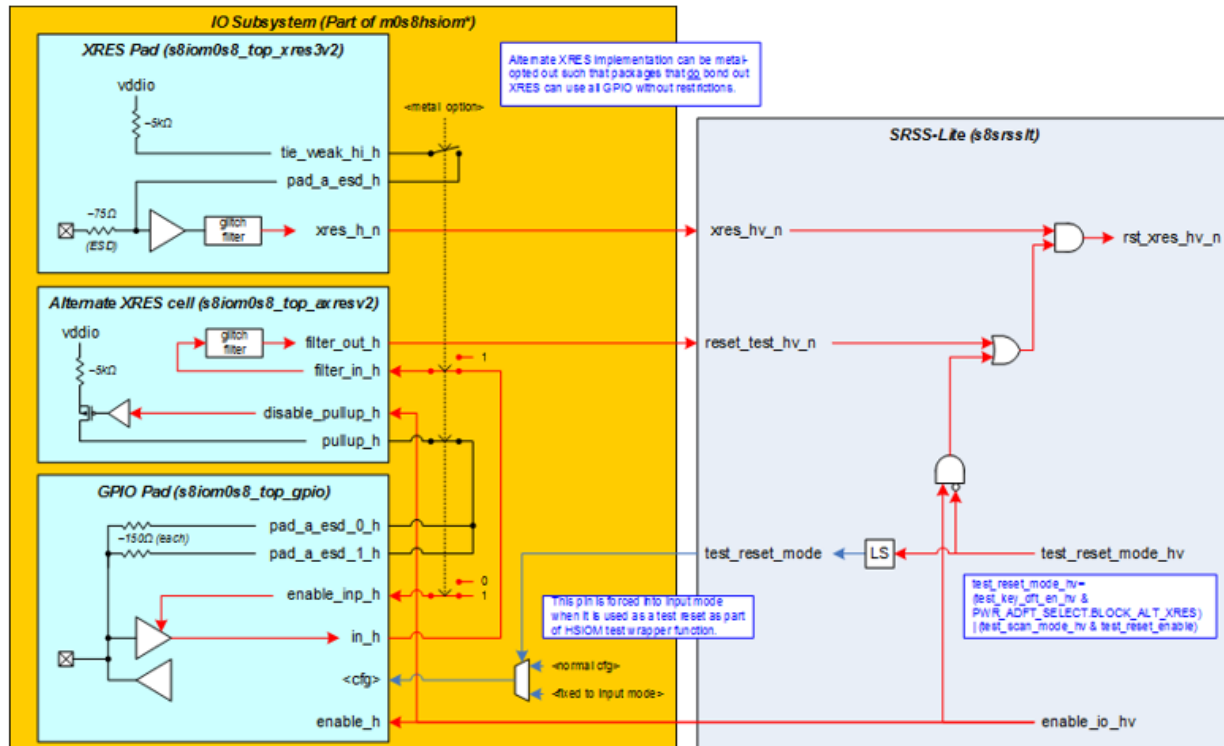
Fig. 6.14: Use case for the XRES cells

sky130_fd_io__top_xres_2:

This is a generic cell that can be abutted to most of the existing cells inside the sky130_fd_io library.

sky130_fd_io__top_xres2v2, sky130_fd_io__top_xres3v2, sky130_fd_io__top_axresv2:

All the sky130_fd_io__top_xres cells have the I/O bussing running through them in M5/M4, thereby forming an I/O ring when abutted to each other. This is a generic cell that can be abutted to most of the existing cells inside the sky130_fd_io library.

Test Pads (TP1, TP2, TP3)

Todo: None of the test pads (TP1, TP2, TP3) is currently publicly available.

TP1 and TP2 are used to monitor the flash voltages. TP3 is an analog pad. The TP1 and TP2 pads do not have any state elements and have no initialization requirements. It is expected that `en_tp1` and `en_tp2` input will be driven low during startup and during normal operation - only toggling high during test modes (class test or characterization, in particular).

The TP1 and TP2 pad are specifically for test mode.

There are two modes: `en_tp1` and `en_tp2` = 0 and `en_tp1` and `en_tp2` = 1.

The `en_tp1` and `en_tp2` inputs must be asserted high to enable scaled/divided version of outputs for full-chip hook-up. In this mode the `tp1_out` voltages and `tp2_out_voltages` are directly observed on the TP1 and TP2 pads.

The TP1, TP2, TP3 pads have snap back ESD protection inside them.

Below are the truth tables for the TP1, TP2, TP3 pads:

Table 6.24: Truth Table for sky130_fd_io__top_tp1

en_tp1	tp1	tp1_div
0	tp1_out	Hi-Z
1	tp1_out	tp1_out/7

Table 6.25: Truth Table for sky130_fd_io__top_tp2

en_tp2	tp2	tp2_div
0	tp2_out	Hi-Z
1	tp2_out	tp1_out/9 + (8/9)*vccd

Table 6.26: Truth Table for sky130_fd_io__top_tp3

tp3	tp3_out
0	0
1	1
Hi-Z	Hi-Z

Overlay Cells

There are two kinds of overlays that exist in the sky130_fd_io I/O library:

- Power Ground (PG) overlays - These overlay cells (12) are coupled with the existing generic power and ground public cells and made into a specific power and ground pad. The overlays connect the pad to the one of the horizontally running I/O ring busses.

- sky130_fd_io__gpio

1. Power Ground Overlays

   sky130_fd_io I/O library has twelve overlays that go with the two existing power and ground pads. The purpose of the overlays is to convert a generic power/ground pad to a specific power/ground pad. For example: sky130_fd_io__top_power_hvc_wpad is just a power pad with no hook-up to the horizontally running I/O busses in the I/O ring. By placing an overlay called sky130_fd_io__overlay_vddio_hvc on top of sky130_fd_io__top_power_hvc_wpad, this would become a VDDIO power pad (in that the PAD is physically connected to the VDDIO bus in the I/O ring).

   Below are the important busses running in the I/O ring for which these overlays are built:

   1. VDDIO

   2. VSSIO

   3. VDDA

   4. VSSA

   5. VCCD

6. VSSD

Since any power or ground pad can be connected to an ESD HV or an ESD LV clamp, there are twelve overlays for the above mentioned buses. Section 6.1.6 shows the usage.

Table 6.27: Overlay Cell along with usage

S.No	Overlay	Used in conjunciton with	Converts above power PAD to	Using underneath clamp of
1	sky130_fd_io__overlay_vc	sky130_fd_io__top_power_h	VDDIO power pad	HV ESD clamp
2	sky130_fd_io__overlay_vc	sky130_fd_io__top_power_lv	VDDIO power pad	LV ESD clamp
3	sky130_fd_io__overlay_vc	sky130_fd_io__top_power_h	VDDA power pad	HV ESD clamp
4	sky130_fd_io__overlay_vc	sky130_fd_io__top_power_lv	VDDA power pad	LV ESD clamp
5	sky130_fd_io__overlay_vc	sky130_fd_io__top_power_h	VCCD power pad	HV ESD clamp
6	sky130_fd_io__overlay_vc	sky130_fd_io__top_power_lv	VCCD power pad	LV ESD clamp
7	sky130_fd_io__overlay_vs	sky130_fd_io__top_ground_l	VSSIO power pad	HV ESD clamp
8	sky130_fd_io__overlay_vs	sky130_fd_io__top_ground_l	VSSIO power pad	LV ESD clamp
9	sky130_fd_io__overlay_vs	sky130_fd_io__top_ground_l	VSSA power pad	HV ESD clamp
10	sky130_fd_io__overlay_vs	sky130_fd_io__top_ground_l	VSSA power pad	LV ESD clamp
11	sky130_fd_io__overlay_vs	sky130_fd_io__top_ground_l	VSSD power pad	HV ESD clamp

Power detector

Todo: sky130_fd_io__top_pwrdet is not yet publicly available.

This cell is developed to detect vddd and vddio power supplies and to level shift the hv control signals across vddio<->vddd voltage domains. This cell is made of the following sub-blocks.

1. vddd detector : It detects the presence of vddd supply in vddio domain

2. vddio detector : It detects the presence of vddio supply in vddd domain

3. There are 6 level shifters inside the top cell. The first 3 level shifters are enabled by the vddd detector and the later three are enabled by the vddio detector. The detectors make sure that the level shifters are powered down to a safe state when the input power supply to the level shifters is not present.

Use case for the detector

Block diagram

The following diagram shows the complete sub-blocks of the power detector in detail.
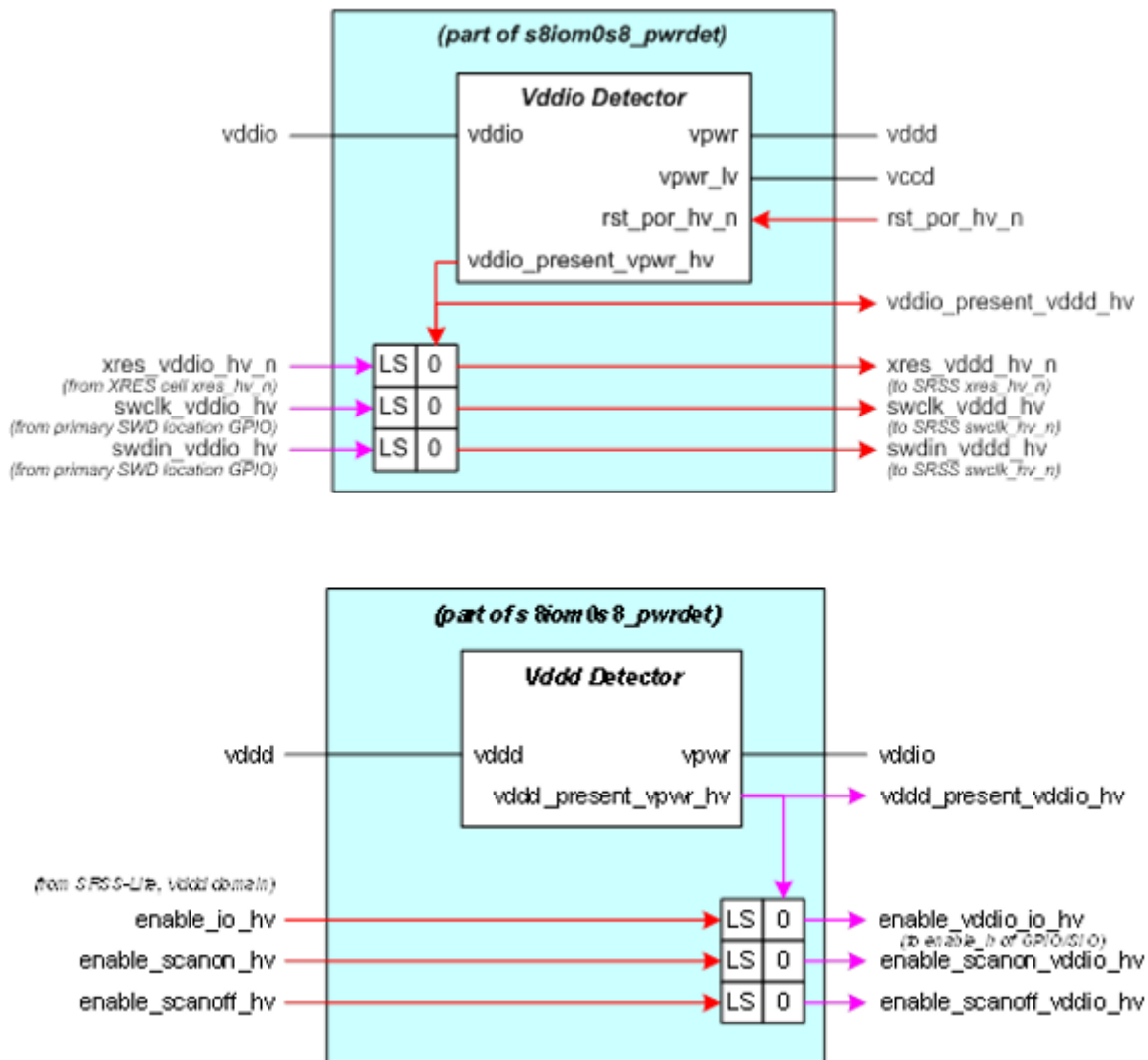
Fig. 6.15: Use case for the Power detector

Fig. 6.16: sky130_fd_io__top_pwrdet

Truth Table

The table below captures all steady state combinations of `vddio_q,` vccd and vddd1 for the vddio detector and explains the behavior of the vddio detector for each of the cases.

Table 6.28: Truth Table for Power detector

vccd	vddd1	vddio_q	vddio detector behavior	Comment
0	0	0	Output is floating.	Chip shutdown
0	0	1	Output is floating.	vddd is absent
0	1	0	The detector is unreliable in this condition	Sec.2.4.9 of SAS calls out this condition. It states the circuit above is unreliable when vddio is 0 and `vpwr_lv` is 0, which is the case during POR and when XRES=0
0	1	1	• Detector output will be high. • vccd=0 does not affect circuit behavior when vddio=1	xres mode
1	0	0	Output is floating.	Invalid combination. Vccd cannot be 1 when vddd is 0
1	0	1	Output is floating.	Invalid combination. Vccd cannot be 1 when vddd is 0
1	1	0	Output will be low. since `vddio_q=0`	When vddio deasserts in a working system - it what leads the system to reset as a result of it
1	1	1	Output of detector is high.	Active mode.

The table below captures all steady state combinations of `vddio_q,` and vddd2 for the vddd detector and explains the behavior of the vddd detector for each of the cases.

Table 6.29: Steady state combinations of `vddio_q,` and vddd2

vddio_q	vddd2	vddd detector behavio	Comment
0	0	Output is floating.	Chip shutdown
0	1	Output is floating	`vddio_q` (power supply of detector) is absent.
1	0	Output will be low, since vddd2 =0	`vddio_q` is present and vddd2 is absent.
1	1	Output will be high, since vddd2=1	Active mode.

The output of the level shifter will be zero when the power supply that is being detected is not present (=0).

Block Integration Guidelines

The cell uses metal routing untill Met3. Met4 and Met5 can be routed above this block.

The `rst_por_hv_n` pin should be hooked up to the `rst_por_hv_n` coming from the SRSS IP for proper functionality.

The cell does not include any circuitry for test mode control or for self-test.

IP block test coverage goals should be met by asserting the inputs of the level shifter and observing the respective outputs. The block is mainly used to carry global enable signals and hence this functionality is tested implicitly.

The detector outputs are buffered using buffer sizes similar to buf4 cell. The user must insert an additional buffer if one intends to cater to a higher load than that is supported by this buffer.

The level shifter outputs are buffered to drive a 3pf load at about 10ns rise/fall times. Any additional load requirement must be taken care by inserting additional buffers.

The reset signal connected to vddio detector should be high in steady state condition for proper functionality.

If the VDDD detector is not to be used then the vddd2 has to be tied to `vddio_q.` The inputs of the corresponding level shifters (`in1_vddd_hv, in2_vddd_hv` and `in3_vddd_hv` must be tied to ground. The outputs of the level shifters and detector must not be used anywhere.

If the VDDIO detector is not planned to be used then the vddd1, `rst_por_hv_n` and vccd has to be tied to `vddio_q.` The inputs of the corresponding level shifters (`in1_vddio_hv, in2_vddio_hv` and `in3_vddio_hv` must be tied to ground. The outputs of the level shifters and detector must not be used anywhere.

This cell can be placed in critical corner.

The cell has power connections in Met3. The power connections must be properly connected in Met4 and Met5 at the chip level. The MET4 and MET5 power hookups should be at least 6um. Minimum 10 VIA3 and VIA4 must be used in the power hookups.

If the block is placed in the I/O ring in the ESD routing path the power bussing should follow that of the I/O ring.

The vddio and vddd detectors were tested with 500mV, 10ns pulse width noise at 1 MHz and 25 MHz frequencies at the input power supply domain assuming no noise at the output power supply domain.

The vddio and vddd detectors were tested with 500mV, 10ns pulse width noise at 1 MHz and 25 MHz frequencies at the output power supply domain assuming no noise at the input power supply domain.

The vddio and vddd detectors were tested with 100mV, 10ns pulse width noise at 1 MHz and 25 MHz frequencies at the vssa domain.

The vddio and vddd detectors were tested with 100mV, 10ns pulse width noise at 1 MHz and 25 MHz frequencies at the vssd and `vssio_q` domain.

The outputs of the level shifters should be routed in Met2 of 0.5um width or Met3

The default state of the level shifters outputs is zero. Hence the level shifters must be used to shift active high control signals to avoid glitches on this control signals during various power supply ramps.

The power detector carries the `enable_io` signals to the sky130_fd_io__sio and sky130_fd_io__gpio_ovtv2. Hence any glitches on the VDDD level shifter output when VDDIO ramping will cause a possible glitch in I2C communication. The following table shows the outputs with various power supply ramp scenarios for the detector and level shifters outputs with the input to the level shifter driven by zero.

Table 6.30: Power detector outputs with various power supply ramp scenarios

Case #	vddd	vddio	vddio detector output	vddio Level shifter output	vddd detector output	vddd Level shifter output
1	Stable	Ramping	no glitch	no glitch	glitches	no glitch
2	Ramping	Stable	glitches	no glitch	no glitch	no glitch
3	Stable	Stable	no glitch	no glitch	no glitch	no glitch
4	Ramping	Ramping	glitches	glitches	glitches	glitches

Case 1: vddio ramp - vddd detector

VDDIO detector is keeping system in reset, so `enable_` signals are 0. Hence LS input is being driven by 0, so a glitch on VDDD detector output is of no concern.

Case 2: vddd ramp - vddio detector

The system is not listening to output of VDDIO detector/level shifter when vddd ramps. Hence this is not a concern.

Case 3: No concerns

Case 4: Glitches on detector/level shifter outputs not a problem during concurrent ramps.

The user must connect the power and ground to the less noisy sources.

sky130_fd_io Pin Information

Todo: sky130_fd_io__gpio is not yet available.

1. DFT, BIST Pins

   As a summary, there is no additional DFT circuitry needed to test the sky130_fd_io__gpio. However, DFT circuitry has been added to the sky130_fd_io__sio macro to test the references from the sky130_fd_io__refgen to the sky130_fd_io__sio macro.

2. Bulk Pins

   There are no bulk pins to the LV devices in this library.

   Some high voltage pfet bodies are connected to their sources. These pfet bodies are connected to the I/O supply `vddio`. There are some high voltage pfet bodies that are associated with the pad during an overvoltage or hot swap event. When a hot swap or overvoltage event occurs, these bodies are connected to the pad otherwise they are connected to the I/O supply `vddio`.

   There are nfet bodies that do not connect to common ground. These bodies are in an isolated psub and are connected to `vssd`. This is required in order to ensure that the threshold voltage does not change if substrate bias

is applied. Normally, this scheme is used in the input buffer to ensure that the input trip does not shift due to substrate biasing.

3. Power Supply Pins

- The sky130_fd_io__gpio cells use the main Vddio/Vssio connections for their ESD current steering diodes.

- The main Vddio/Vssio power rails are used for the digital output driver only. A separately routed `Vddio_quiet`/ `Vssio_quiet` bus is used for all lower current circuits.

- Most LV logic is in the Vccd domain. A few signals are in the Vcchib domain to enable DeepSleep functionality.

- The AMUXBUS section contains switches that are supplied from the Vdda domain. The gates are driven using the Vswitch supply, which is either equal to Vdda or pumped up from it. If the product has no Programmable Analog, these supplies can be connected to Vddio (e.g. TSGx).

- The AMUXBUS section contains shunting switches to Vssio/Vddio for the sensing/shielding currents during CSD operation. These use the `Vssio_quiet`/`Vddio_quiet` rails with private routes to the corresponding Vssio/Vddio pads to minimize the noise experienced due to IR- Drop caused by switching current of regular digital drivers.

- There are no control signals in the Vdda domain. Only the AMUXBUS buses themselves are in the Vdda domain.

Timing Requirements and Diagrams

The following diagrams apply to the input buffer AC parameters.
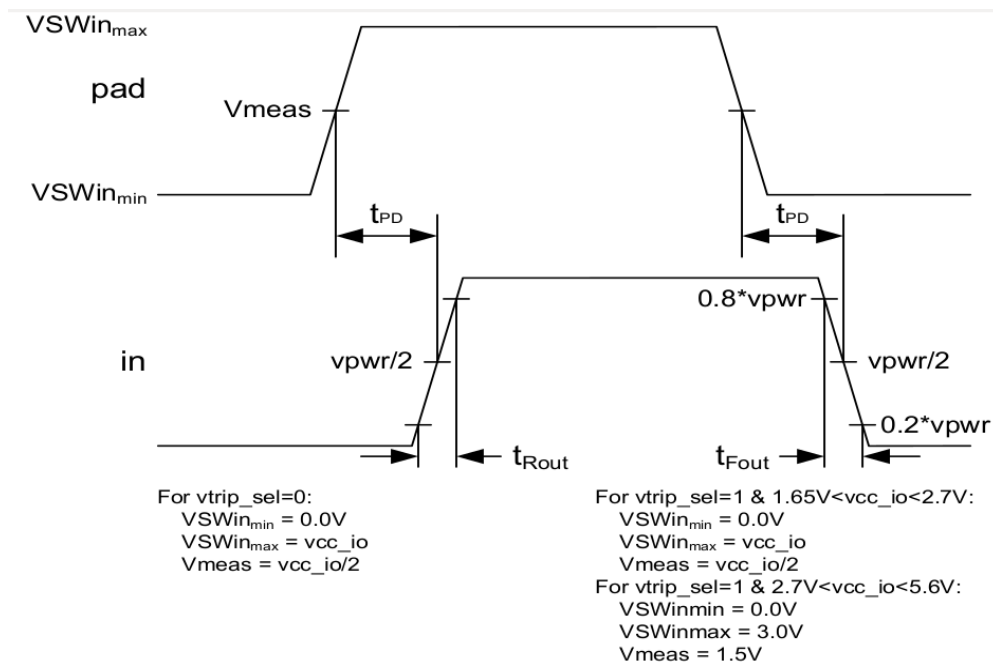
Fig. 6.17: sky130_fd_io__gpio, tPD, tRFout

The following timing diagrams apply to the output buffer AC parameters.
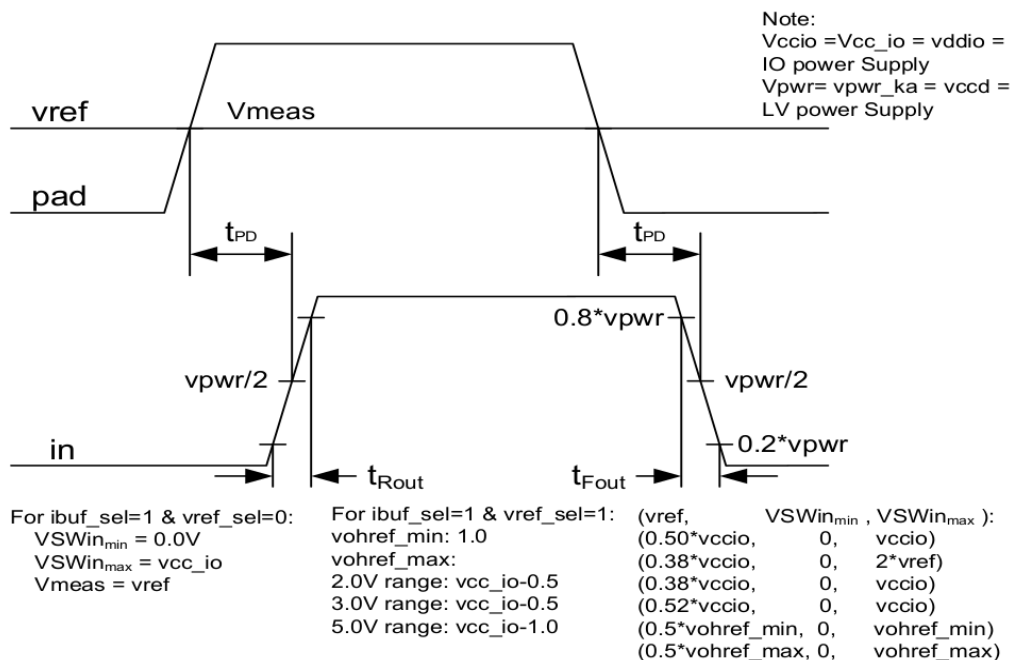
Fig. 6.18: sky130_fd_io__sio tPD, tRFout
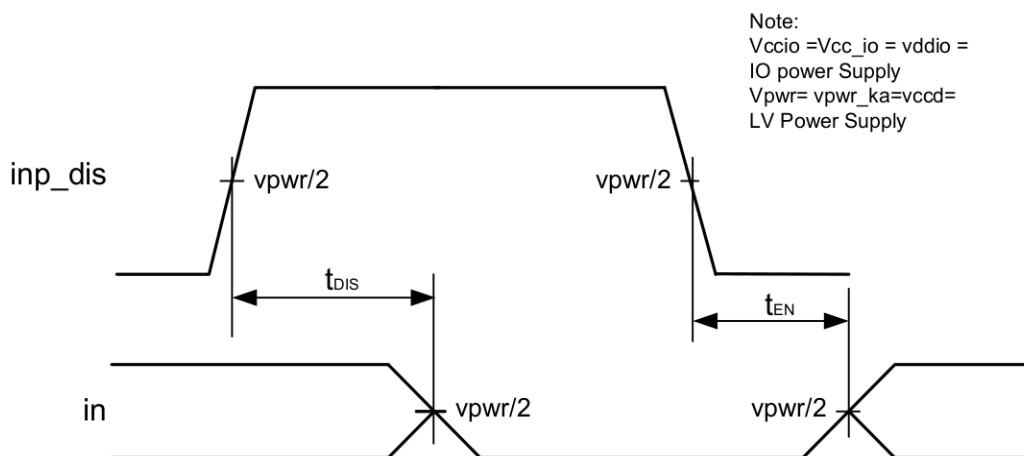
Fig. 6.19: sky130_fd_io__gpio & sky130_fd_io__sio tDIS, tEN
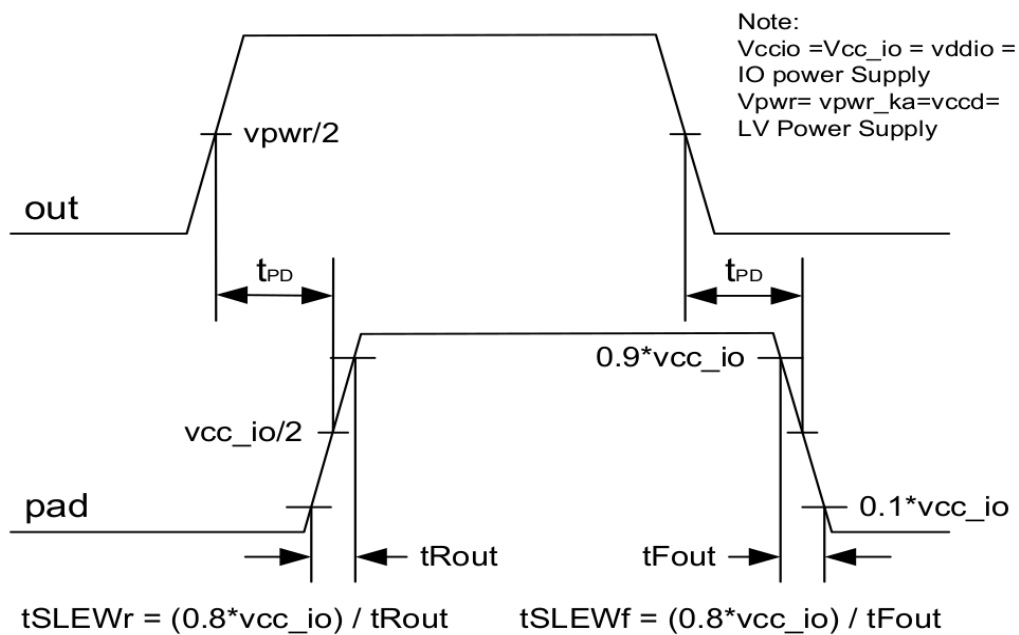
Fig. 6.20: sky130_fd_io__gpio tPD, tRFout (tSLEW)
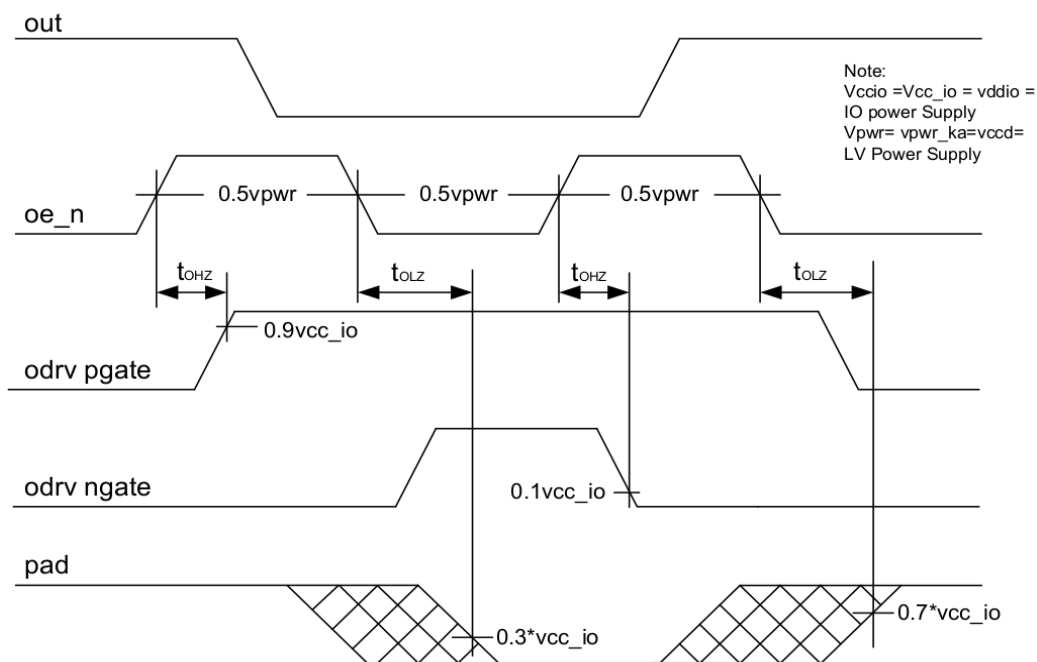
Fig. 6.21: sky130_fd_io__gpio and sky130_fd_io__sio non-regulated outbuf tOLZ & internal measurement method for tOHZ
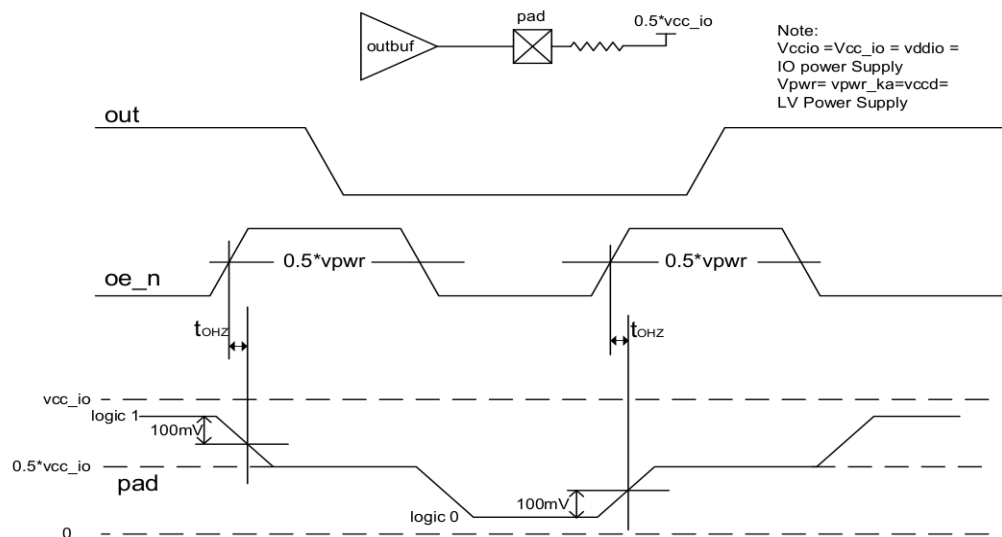
Fig. 6.22: sky130_fd_io__gpio and sky130_fd_io__sio non-regulated outbuf tOHZ external measurement method
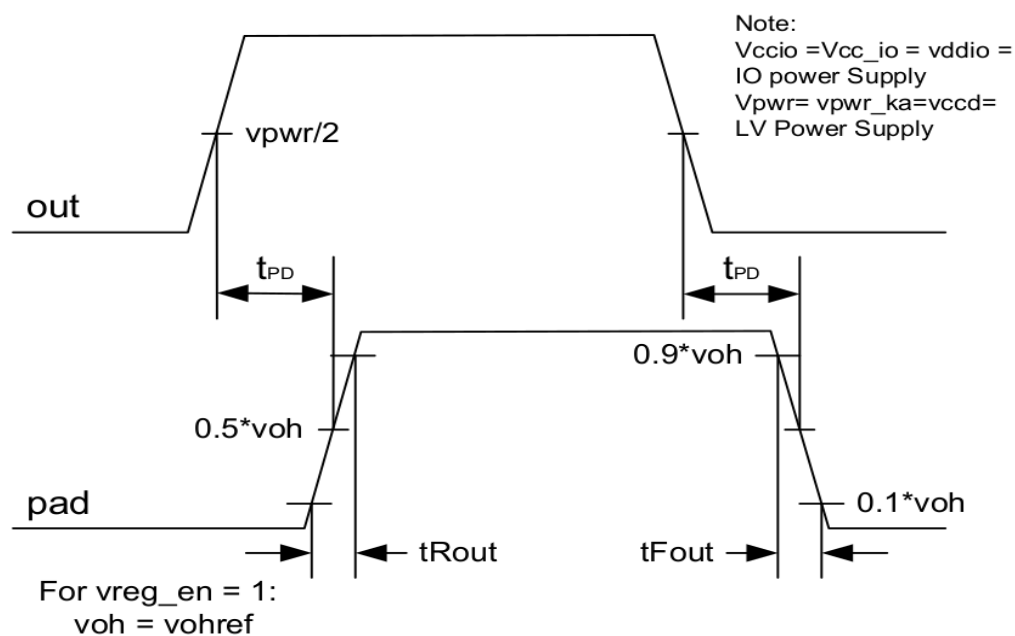
Fig. 6.23: sky130_fd_io__sio regulated outbuf ttRFout(tSLEW)
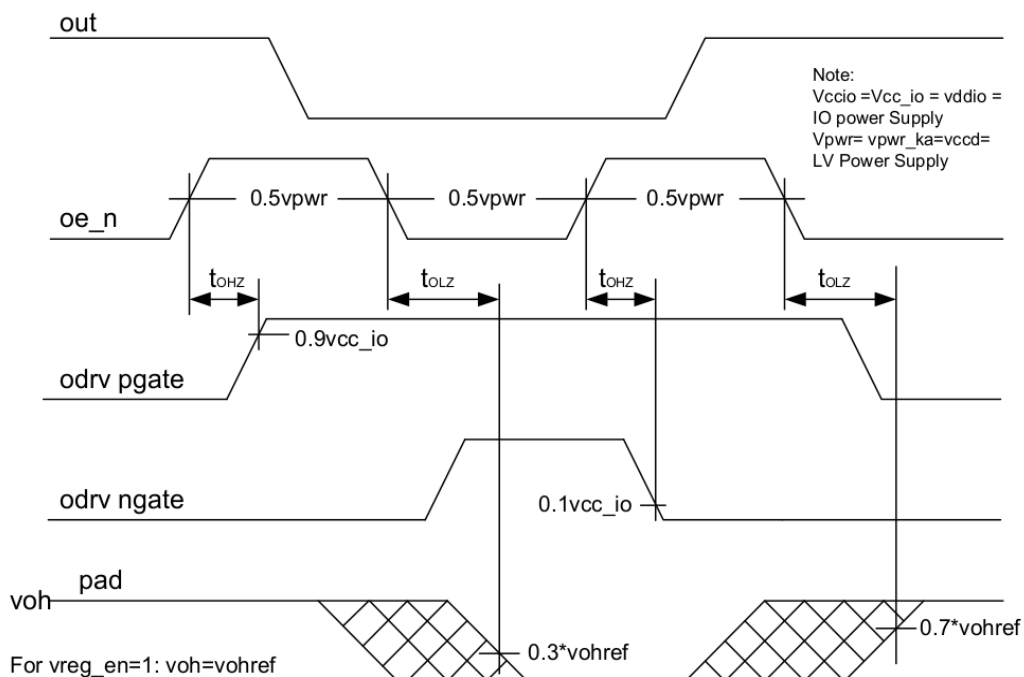
Fig. 6.24: sky130_fd_io__sio regulated outbuf tOLZ & external measurement method for tOHZ
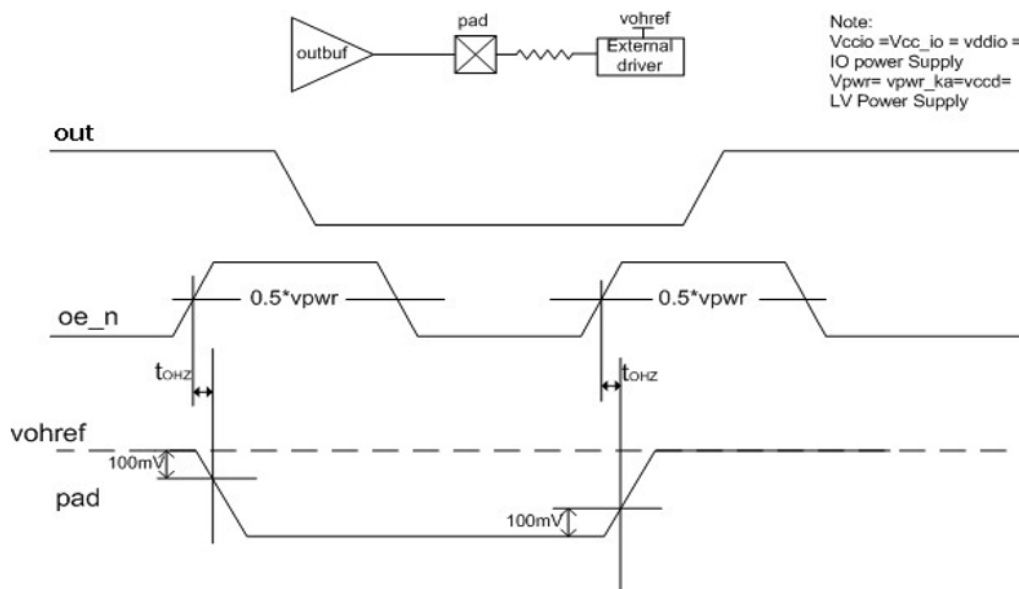
Fig. 6.25: sky130_fd_io__sio regulated outbuf tOHZ external measurement method
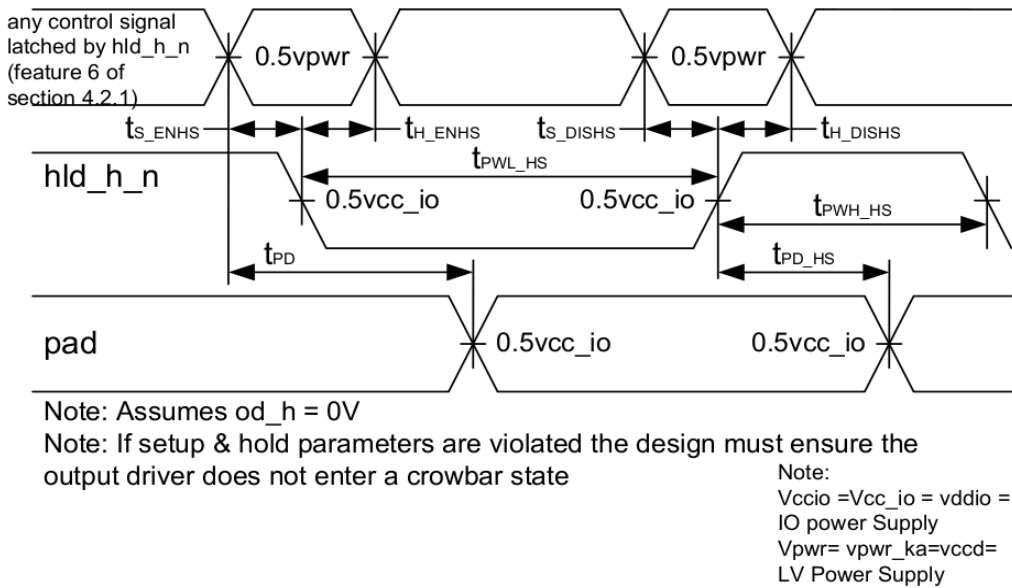
Fig. 6.26: sky130_fd_io__gpio and sky130_fd_io__sio Hold State Mode Timing Diagram

Block Level Interfaces

The sky130_fd_io__gpio and sky130_fd_io__sio cells interface with the core and the external world. These cells accept inputs from the core at `vcchib`, `vccd`, `vdda` and `vddio` voltage levels. The cell interfaces with the external world at `vddio` and `vdda` levels. This cell also produces output signals to the core at `vcchib` and `vddio` levels. `vcchib` tracks vccd in normal operation and does not track `vccd` in sleep mode in which `vddio` and `vcchib` are up and `vccd` is down.

The sky130_fd_io__sio_macro cell is like the sky130_fd_io__gpio cell and it also accepts analog voltage levels as inputs and produces analog voltages at the pad.

The internal blocks on the `vcchib` power domain are input buffers and control logic for `oe_hs` (hot swap output enable).

The Reference voltage generator block receives the vohref analog global signal and has low voltage input configuration signals (`vreg_en`, `vref_sel` , `ibuf_sel` , `vtrip_sel`). This block provides `voutref` reference voltage and `refleak_bias` bias voltage for the sky130_fd_io__sio Regulated Output Buffer and the `vinref` reference voltage for the sky130_fd_io__sio differential input buffer. The internal blocks on the `vcchib` power domain is the internal current bias generator and a level shifter block, that controls that sub-block.

The Reference voltage generator `vcc_a` pin must be connected to the analog supply of the chip, to reduce its noise sensitivity at its Vinref and Voutref outputs. This issue affects the supply noise sensitivity in the sky130_fd_io__sio input buffer and the sky130_fd_io__sio Regulated Output Buffer, respectively.

Reset and Initialization

There are two resets to the I/O blocks -

- `Enable_h` - This is a reset issued by the SRSS in VDDD (VDDIO) domain that resets everything when it is at logic 0 in the I/O block and ensures that the I/O blocks are tri-stated

- `Enable_vdda_h` - This is reset issued by the SRSS in VDDA domain to ensure that any analog blocks in VDDA domain are reset when `enable_vdda_h` is at logic 0. This will ensure that any portions of the I/O (Analog Mux) that are tied to PAD are reset and the I/O block is in reset state.

Power Modes

Todo: sky130_fd_io__gpio is not yet available.

The sky130_fd_io__gpio and sky130_fd_io__sio buffers support multiple standby modes. The following tables list the input and output standby modes and their dependency on the related control inputs.

Table 6.31: sky130_fd_io__gpio & sky130_fd_io__sio Input Buffer Standby Modes

enable_h	inp_dis	dm<2:0>	Standby Mode Description
1	X	000	Input Buffer disabled by drive mode state
1	1	XXX	Input Buffer disabled by input buffer disable input
0	X	XXX	Input Buffer disabled

Table 6.32: sky130_fd_io__gpio & sky130_fd_io__sio Output Buffer Standby Modes

enable_h	hld_h_n	oe_n	dm<2:0>	Standby Mode Description
1	1	X	00X	Output Buffer disabled by drive mode state
1	1	1	• 1XX • X1X	Output Buffer disabled by output buffer enable signal
1	0	X	XXX	Output Buffer maintains previous state
0	X	X	XXX	Output Buffer tri-stated

The standby power consumption depends on the state of the control bits. For example, the lowest standby current mode is achieved when oe_n=1, inp_dis=1, dm<2:0>=000. During this mode the input and output buffer are permanently disabled allowing the circuits to be configured for minimal leakage current.

For all control bit states not covered in Table 6.30 and Table 6.31 either the input buffer, output buffer, or both buffers will be enabled. During these modes the I/O buffer is considered active. The power consumption for these modes depends on the drive mode setting and the switching frequency.

Register Definitions

This IP contains latches to hold the previous state of the output when the hold state mode is selected. When the hold state mode is selected the internal power supply connected to the output path may float. The hold state latches are required to hold the previous output state regardless of the current state of the control signals.

Power Architecture and Modes

The IP cells include multiple power domains. In general there is a high voltage domain and a low voltage domain. The high voltage domain is supplied by the I/O power supply `vddio`. There are no switched domains located inside the cell for the `vddio` power supply domain.

The low voltage domain consists of two internally generated supplies, vccd and vcchib. The vccd supply is the regulated internal supply that can be forced low during low standby current modes. The vcchib supply is the low voltage regulated keep alive supply. This supply is kept active during low standby current modes and the level can drop to 1.2V. The chip team is responsible to correctly controlling the levels on these supplies during the appropriate modes of operation.

Grounded Power Supplies

As there are multiple power supplies to the I/O's, no single power supply will be grounded while another supply is active. This will help alleviate the grounded NWELL issues that induce latch-up. It is OK to float a supply while another is active though.

Block behavioral model requirements

Todo: sky130_fd_io__gpio is not yet available.

The sky130_fd_io__gpio and sky130_fd_io__sio input buffers are operating from the vcchib supply. This means that the input buffer can operate even when vccd is taken down to 0 or floats. But, note that before taking vccd=0 (or floating vccd), the hold mode must be asserted i.e. hld_h_n=0 must go to 0 before vccd is taken to 0. During the hold mode of operation and with vccd=0 (or floating), the input buffer can actively drive out depending on pad input if there is a valid I/O (vddio, vddioq and vcchib) power supply. This functionality is implemented in the behavioral model. If vccd=0 (or floats) and when the I/O is not in the hold mode of operation, the behavioral model would force an `X` on the outputs of the input buffer (`out` and `out_h`) and the input buffer cannot be actively driven from pad.

Block Integration Requirements and Constraints

General Integration Requirements

Todo: Only sky130_fd_io__gpiov2 and sky130_fd_io__gpio_ovtv2 are currently available. sky130_fd_io__gpio is not yet publicly available.

Todo: Only sky130_fd_io__top_xres4v2 is currently available. sky130_fd_io__top_xres, sky130_fd_io__top_xres_2, sky130_fd_io__top_xres2v2, sky130_fd_io__top_xres3v2, and sky130_fd_io__top_axresv2 are not yet available.

The following is a list of items users must be aware of before using this IP.

1. The IP cells described within this document are I/O cells and Power and Ground pads. Each cell (GPIO and sky130_fd_io__sio) contains an input and output buffer, with a bond pad.

2. The circuit blocks do not include any circuitry for test mode control or for self-test. All input pin states will be exercisable in all product applications so that the IP block test coverage goals will be met.

3. The control signal `enable_h` will override all other input and control pins to force the input and output to a predetermined state. When `enable_h` transitions from logic 0 to logic 1, the block expects all of the inputs to be valid state. If `hld_h_n=0` when the `enable_h` pin transitions 0->1 (inactive->active) the state set by `enable_h` is latched in the output driver.

4. There is a separate `enable_vdda_h` control signal to the sky130_fd_io__gpio. This control signal is logic 0 when VDDA supply is ramping up. This control signal ensures that the AMUX is completely turned OFF when `enable_vdda_h` is at logic 0.

5. It is permissible to externally connect the I/O pin to a voltage above vddio or below `vssd_io`, provided that the current flowing into/out of the pin is externally limited to 100uA.

6. The sky130_fd_io__gpio and sky130_fd_io__sio input buffers are operating from the vcchib supply. This means that the input buffer can operate even when vccd is taken down to 0V or floats. But note that before taking vccd=0 (or floating vccd), the hold mode must be asserted i.e. `hld_h_n=0` must go to 0 before vccd is taken to 0. During the hold mode of operation and with vccd=0 (or floating), the input buffer can actively drive out depending on pad input if there is a valid I/O (vddio, vddioq and vcchib) power supply. This functionality is implemented in the behavioral model. If vccd=0 (or floats) and when the I/O is not in the hold mode of operation, the behavioral model would force an `X` on the outputs of the input buffer (`out` and `out_h`) and the input buffer cannot be actively driven from pad.

7. In hibernate mode, the I/P buffer just needs to toggle. It need not meet the VIH/VIL specs.

8. The charge pump is powered down during startup and thus VSWITCH=VDDA during startup.

9. `tie_weak_hi_h` signal for the sky130_fd_io__top_xres3v2 is really a pull up and not intended to interact with any other intermediate strength drivers (weak, pull).

10. For the cell sky130_fd_io__top_axresv2, glitch filter input (`filter_in_h`) is intended to be connected to only the sky130_fd_io__gpio output and no other uses are permitted.

11. The glitch filter in sky130_fd_io__top_xres2v2, sky130_fd_io__top_xres3v2 and sky130_fd_io__top_axresv2 cells have metal1 option to increase/decrease the glitch rejection pulse width.

12. When using the pad connections of the sky130_fd_io__sio_macro, care should be taken about power-domain interaction at PAD (when used as I2C pads). The sky130_fd_io__sio_macro has a tracking NWELL on its PAD which is driven to VDDIO when PAD<VDDIO. If a pad is being connected to a signal from any other power-domain other than VDDIO, power- supply sequencing issues must be analyzed at chip- level.

1. Chip Floor planning guidelines when using sky130_fd_io to build I/O ring

    The following information is a MUST know when using the sky130_fd_io library components to build an I/O ring. Due to the complex nature of these I/O's and other PG pads, it is critical that the following matrix be understood when placing the cells that form the I/O ring.

    - ALL cells CANNOT be abutted with each other. There are limitations because of the ESD LU rules and due to the different Deep NWELLS being used in different cells.

    - It is strongly recommended to run a DRC at the chip level as soon as the I/O cell placements are complete. Also, scheduling a preliminary ESD review is recommended before routing is started.

2. Layout Integration guidelines specific to sky130_fd_io__gpio

    1. The GPIO cell (sky130_fd_io__top_gpio) forms part of the I/O ring. If multiple instances of this cell are used, they must be mirrored and placed by abutment.

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2. The boundary of the sky130_fd_io__gpio cell (PAD side) can be abutted with the seal ring. It takes care of the pad to seal ring rules internally.

3. The sky130_fd_io__gpio cell can be abutted to the rest of the cells in this IP by proper placement as documented below for the rest of the public cells.

3. `enable_h` integration guidelines for sky130_fd_io__gpio_ovtv2 and sky130_fd_io__sio_macro

Any product that has I2C ports and is claiming over-voltage tolerance needs to ensure that the glitch on `enable_h` coming into the sky130_fd_io__top_gpio_ovtv2 or sky130_fd_io__sio_macro is less than 300mV.

Scan Attributes to be used for sky130_fd_io cells

Todo: sky130_fd_io__gpio and sky130_fd_io__top_amuxsplitv2 are not yet available.

sky130_fd_io__gpio's can be used as SCAN IN and SCAN Out pads based on the configuration.

However, if a sky130_fd_io__gpio is configured as a SCAN IN pad, all the output buffer control signals can be toggled. Likewise, if the sky130_fd_io__gpio is used as a SCAN OUT pad, all the input buffer control signals can be toggled.

Table 6.33: Control signals that can be toggled for public cells

S.No	Public Cell	• Used as SCAN IN • dm[3]=001 • analog_en=0	• Used as SCAN OUT • dm=110 • inp_dis=1 • analog_en=0	• Others • analog_en=0 • hld_vdda_h_n=0
1	sky130_fd_io__top_g	• out • oe_n • slow • analog_sel • analog_pol	• vtrip_sel ib_mode_sel • analog_sel analog_pol	
2	sky130_fd_io__top_g	• out • oe_n • slow • analog_sel • analog_pol • hys_trim • slew_ctl<1:0	• vtrip_sel • ib_mode_sel< • analog_sel • analog_pol • hys_trim • slew_ctl<1:0	
3	sky130_fd_io__sio_m (assuming both the pad in macro are used the same way)	• inp_dis=0 • vtrip_sel=0 • hld_h_n=1 • ibuf_sel=0 • vreg_en_refg • out<1:0> • oe_n<1:0> • slow<1:0> • voh_sel<1:0> • vref_sel<1:0 • vtrip_sel_re • ibuf_sel_ref • dft_refgen=0	• vreg_en=0 • vreg_en_refg • vtrip_sel<1: • ibuf_sel<1:0 • voh_sel<2:0> • vref_sel<1:0 • vtrip_sel_re • ibuf_sel_ref • dft_refgen=0	
4	sky130_fd_io__top_a			• switch_aa_sl • switch_aa_sr • switch_aa_s0 • switch_bb_sl • switch_bb_sr • switch_bb_s0

Chapter 6. PDK Contents

Third party provided IO and Periphery Libraries

Cells in libraries cross-index

Cell name	hd	hdll	hs	io	ls	ms	Number of libraries
a2111o	x		x		x	x	4
a2111oi	x		x		x	x	4
a211o	x	x	x		x	x	5
a211oi	x	x	x		x	x	5
a21bo	x	x	x		x	x	5
a21boi	x	x	x		x	x	5
a21o	x	x	x		x	x	5
a21oi	x	x	x		x	x	5
a221o	x		x		x	x	4
a221oi	x	x	x		x	x	5
a222o			x		x	x	3
a222oi	x	x	x		x	x	5
a22o	x	x	x		x	x	5
a22oi	x	x	x		x	x	5
a2bb2o	x	x	x		x	x	5
a2bb2oi	x	x	x		x	x	5
a311o	x		x		x	x	4
a311oi	x		x		x	x	4
a31o	x	x	x		x	x	5
a31oi	x	x	x		x	x	5
a32o	x	x	x		x	x	5
a32oi	x	x	x		x	x	5
a41o	x		x		x	x	4
a41oi	x		x		x	x	4
and2	x	x	x		x	x	5
and2b	x	x	x		x	x	5
and3	x	x	x		x	x	5
and3b	x	x	x		x	x	5
and4	x	x	x		x	x	5
and4b	x	x	x		x	x	5
and4bb	x	x	x		x	x	5
buf	x	x	x		x	x	5
bufbuf	x	x	x		x	x	5
bufinv	x	x	x		x	x	5
clkbuf	x	x	x		x	x	5
clkdlybuf4s15	x						1
clkdlybuf4s18	x						1
clkdlybuf4s25	x						1
clkdlybuf4s50	x						1
clkdlyinv3sd1			x		x	x	3
clkdlyinv3sd2			x		x	x	3
clkdlyinv3sd3			x		x	x	3
clkdlyinv5sd1			x		x	x	3
clkdlyinv5sd2			x		x	x	3
clkdlyinv5sd3			x		x	x	3
clkinv	x	x	x		x	x	5

Table 6.34 – continued from previous page

Cell name	hd	hdll	hs	io	ls	ms	Number of libraries
clkinvlp	x	x					2
clkmux2		x					1
conb	x	x	x		x	x	5
decap	x	x	x		x	x	5
decaphe					x		1
decaphetap					x		1
dfbbn	x		x		x	x	4
dfbbp	x		x		x	x	4
dfrbp	x		x		x	x	4
dfrtn	x		x		x	x	4
dfrtp	x	x	x		x	x	5
dfsbp	x		x		x	x	4
dfstp	x	x	x		x	x	5
dfxbp	x		x		x	x	4
dfxtp	x		x		x	x	4
diode	x	x	x		x	x	5
dlclkp	x		x		x	x	4
dlrbn	x		x		x	x	4
dlrbp	x		x		x	x	4
dlrtn	x	x	x		x	x	5
dlrtp	x	x	x		x	x	5
dlxbn	x		x		x	x	4
dlxbp	x		x		x	x	4
dlxtn	x	x	x		x	x	5
dlxtp	x		x		x	x	4
dlygate4sd1	x	x	x		x	x	5
dlygate4sd2	x	x	x		x	x	5
dlygate4sd3	x	x	x		x	x	5
dlymetal6s2s	x		x		x	x	4
dlymetal6s4s	x		x		x	x	4
dlymetal6s6s	x		x		x	x	4
ebufn	x	x	x		x	x	5
edfxbp	x		x		x	x	4
edfxtp	x		x		x	x	4
einvn	x	x	x		x	x	5
einvp	x	x	x		x	x	5
fa	x		x		x	x	4
fah	x		x		x	x	4
fahcin	x		x		x	x	4
fahcon	x		x		x	x	4
fill	x	x	x		x	x	5
fill_diode			x		x	x	3
ha	x		x		x	x	4
inputiso0n		x					1
inputiso0p		x					1
inputiso1n		x					1
inputiso1p		x					1
inv	x	x	x		x	x	5
isobufsrc		x					1
lpflow_bleeder	x						1

continues on next page

Table 6.34 – continued from previous page

Cell name	hd	hdll	hs	io	ls	ms	Number of libraries
lpflow_clkbufkapwr	x						1
lpflow_clkinvkapwr	x						1
lpflow_decapkapwr	x						1
lpflow_inputiso0n	x						1
lpflow_inputiso0p	x						1
lpflow_inputiso1n	x						1
lpflow_inputiso1p	x						1
lpflow_inputisolatch	x						1
lpflow_isobufsrc	x						1
lpflow_isobufsrckapwr	x						1
lpflow_lsbuf_lh_hl_isowell_tap	x						1
lpflow_lsbuf_lh_isowell	x						1
lpflow_lsbuf_lh_isowell_tap	x						1
macro_sparecell	x						1
maj3	x		x		x	x	4
mux2	x	x	x		x	x	5
mux2i	x	x	x		x	x	5
mux4	x		x		x	x	4
muxb16to1		x					1
muxb4to1		x					1
muxb8to1		x					1
nand2	x	x	x		x	x	5
nand2b	x	x	x		x	x	5
nand3	x	x	x		x	x	5
nand3b	x	x	x		x	x	5
nand4	x	x	x		x	x	5
nand4b	x	x	x		x	x	5
nand4bb	x	x	x		x	x	5
nor2	x	x	x		x	x	5
nor2b	x	x	x		x	x	5
nor3	x	x	x		x	x	5
nor3b	x	x	x		x	x	5
nor4	x	x	x		x	x	5
nor4b	x	x	x		x	x	5
nor4bb	x	x	x		x	x	5
o2111a	x		x		x	x	4
o2111ai	x		x		x	x	4
o211a	x	x	x		x	x	5
o211ai	x	x	x		x	x	5
o21a	x	x	x		x	x	5
o21ai	x	x	x		x	x	5
o21ba	x	x	x		x	x	5
o21bai	x	x	x		x	x	5
o221a	x	x	x		x	x	5
o221ai	x	x	x		x	x	5
o22a	x	x	x		x	x	5
o22ai	x	x	x		x	x	5
o2bb2a	x	x	x		x	x	5
o2bb2ai	x	x	x		x	x	5
o311a	x		x		x	x	4

continues on next page

Table 6.34 – continued from previous page

Cell name	hd	hdll	hs	io	ls	ms	Number of libraries
o311ai	x		x		x	x	4
o31a	x		x		x	x	4
o31ai	x	x	x		x	x	5
o32a	x		x		x	x	4
o32ai	x	x	x		x	x	5
o41a	x		x		x	x	4
o41ai	x		x		x	x	4
or2	x	x	x		x	x	5
or2b	x	x	x		x	x	5
or3	x	x	x		x	x	5
or3b	x	x	x		x	x	5
or4	x	x	x		x	x	5
or4b	x	x	x		x	x	5
or4bb	x	x	x		x	x	5
probe_p	x	x					2
probec_p	x	x					2
sdfbbn	x		x		x	x	4
sdfbbp	x	x	x		x	x	5
sdfrbp	x	x	x		x	x	5
sdfrtn	x	x	x		x	x	5
sdfrtp	x	x	x		x	x	5
sdfsbp	x	x	x		x	x	5
sdfstp	x	x	x		x	x	5
sdfxbp	x	x	x		x	x	5
sdfxtp	x	x	x		x	x	5
sdlclkp	x	x	x		x	x	5
sedfxbp	x	x	x		x	x	5
sedfxtp	x		x		x	x	4
tap	x	x	x		x	x	5
tapmet1			x		x	x	3
tapvgnd	x	x	x		x	x	5
tapvgnd2	x	x	x		x	x	5
tapvgndnovpb					x		1
tapvpwrvgnd	x	x	x		x	x	5
top_gpio_ovtv2				x			1
top_gpiov2				x			1
top_ground_hvc_wpad				x			1
top_ground_lvc_wpad				x			1
top_power_hvc_wpad				x			1
top_power_hvc_wpadv2				x			1
top_power_lvc_wpad				x			1
top_refgen				x			1
top_refgen_new				x			1
top_sio				x			1
top_sio_macro				x			1
top_xres4v2				x			1
xnor2	x	x	x		x	x	5
xnor3	x	x	x		x	x	5
xor2	x	x	x		x	x	5
xor3	x	x	x		x	x	5

6.2 File Types

| File Type | What does it do? | Open Tooling Options | | | | Closed Tooling Options | | | |
		Tool	Status	File format	Source	Tool	Status	File format	Source
Parameterized Cell Generators	Primitive devices that have layouts determined by parameterization.	Magic	Read	TCL script	Hand Written	Cadence Virtuoso	In Progr	Cadence PCells	Hand Written
DRC Deck	Verifies a design meets the design rules	Magic	Read	Magic techfile	Hand Written	Mentor Calibre	In progr	SVRF Rule Decks	Generated from documentation data
LVS Deck	Verifies layout and schematic are equivalent.	Magic	Read	Magic techfile	Hand Written	Mentor Calibre	In progress	SVRF Rule Decks	Generated from documentation data
		Netgen	Read	Netgen setup file	Hand Written				
GDS Generator	Creates mask layout data.	Magic	Read	Magic techfile	Hand designed				
Library Exchange Format Macros	Abstract cell view.	Magic	Read	LEF	Generated from GDS data	?			
Timing Files	Describes pin-to-pin timing	?	Read	Liberty	Generated from JSON data	?			
Netlists	Transistor level circuit description	Ngspi	Read	Ngspice or CDL	?	?	?	OpenAccess?	Generated from spice files
Device Models	Models for use with SPICE	Ngspi	Read	SPICE simulation file	?	Cadence Spectre	In Progr	Spectre?	Generated from spice files
Schematic	Transistor level circuit description	Xcircuit?	None	EDIF	?	Cadence Virtuoso	In Progr	OpenAccess?	?
Schematic Symbol	Symbol for use in schematics	Xcircuit?	None	EDIF	?	Cadence Virtuoso	In Progr	OpenAccess?	?
Verilog testbench	Digital simulation	Icarus Verilog	Read	Verilog	ngsim	Cadence ?	?	OpenAccess?	Generated from Verilog files
XSPICE	Mixed-signal simulation	Ngspi	Read	SPICE	?	?	?	?	?
	Rules for scribe lines and saw lines	?	None	Unknown	?	Cadence ?	In Progr	Cadence SKILL script	Hand written
Param-	Rules for seal ring	Magic	Read	TCL	?	Ca-	In	Ca-	Hand writ-

ANALOG DESIGN

7.1 TODO: analog/virtuoso

7.2 TODO: analog/magic

7.3 TODO: analog/klayout

7.4 TODO: analog/bag

7.5 TODO: analog/fasoc

7.6 TODO: analog/new

EIGHT

DIGITAL DESIGN

8.1 TODO: digital/innovus

8.2 TODO: digital/openroad

8.3 TODO: digital/new

SIMULATION

9.1 TODO: sim/spectre

9.2 TODO: sim/ngspice

Todo: The SkyWater SKY130 PDK provides simulation two types of simulation models. Spectre models for usage with Cadence Spectre and Spice models which are compatible with popular open source spice simulators like *ngspice*.

PHYSICAL & DESIGN VERIFICATION

10.1 Design Rule Verification

10.1.1 TODO: verification/drc/calibre

10.1.2 TODO: verification/drc/magic

10.1.3 TODO: verification/drc/klayout

10.2 Layout verse Schematic (LVS) Verification

10.2.1 TODO: verification/lvs/calibre

10.2.2 TODO: verification/lvs/magic

10.2.3 TODO: verification/lvs/klayout

10.3 Parasitics Extraction (PEX)

10.3.1 TODO: verification/pex/calibre

10.3.2 TODO: verification/pex/magic

10.3.3 TODO: verification/pex/klayout

Todo: The SkyWater SKY130 PDK provides automated physical and design rule checking decks.

These verification rules provide;

- *Design Rule Checking* (*DRC*) against rules described in the *SkyWater SKY130 Process Design Rules* documentation.

> **Warning:** There are some design rules which can not be verified with these decks. They are clearly marked in the *SkyWater SKY130 Process Design Rules* documentation and should be manually verified by the designer.

- *Layout Verse Schematic* (:term`LVS`) Verification

- *Parasitic Extraction* (*PEX*)

10.4 TODO: Calibre Decks

Put stuff here.

10.5 TODO: MAGIC Decks

Put stuff here.

SKYWATER PDK PYTHON API

TODO: Add documentation here

11.1 skywater_pdk package

11.1.1 Submodules

11.1.2 skywater_pdk.base module

class skywater_pdk.base.**Cell**(*name: str*, *library:* Library *| None = None*)

> Bases: `object`
>
> Cell in a library.
>
> **See also:**
>
> *skywater_pdk.base.parse_pathname*, *skywater_pdk.base.parse_filename*, *skywater_pdk.base.*
> *Library*
>
> **Examples**

```
>>> c = Cell.parse("sky130_fd_sc_hd__abc")
>>> c
Cell(name='abc', library=Library(node=LibraryNode.SKY130, source=LibrarySource('fd
↪'), type=LibraryType.sc, name='hd', version=None))
>>> c.fullname
'sky130_fd_sc_hd__abc'
```

```
>>> c = Cell.parse("abc")
>>> c
Cell(name='abc', library=None)
>>> c.fullname
Traceback (most recent call last):
    ...
ValueError: Can't get fullname for cell without a library! Cell(name='abc',␣
↪library=None)
```

> **classmethod from_dict**(*kvs: dict | list | str | int | float | bool | None*, ***, *infer_missing=False*) → A

classmethod from_json(*s: str | bytes | bytearray*, *, *parse_float=None*, *parse_int=None*, *parse_constant=None*, *infer_missing=False*, ***kw*) → A

property fullname

library: *Library* | None = None

name: str

classmethod parse(*s*)

classmethod schema(*, *infer_missing: bool = False*, *only=None*, *exclude=()*, *many: bool = False*, *context=None*, *load_only=()*, *dump_only=()*, *partial: bool = False*, *unknown=None*) → SchemaF[A]

to_dict(*encode_json=False*) → Dict[str, dict | list | str | int | float | bool | None]

to_json(*, *skipkeys: bool = False*, *ensure_ascii: bool = True*, *check_circular: bool = True*, *allow_nan: bool = True*, *indent: int | str | None = None*, *separators: Tuple[str, str] | None = None*, *default: Callable | None = None*, *sort_keys: bool = False*, ***kw*) → str

class skywater_pdk.base.**Library**(*node:* LibraryNode, *source:* LibrarySource, *type:* LibraryType, *name: str = ''*, *version:* LibraryVersion *| None = None*)

Bases: *Library*

Library of cells.

See also:

skywater_pdk.base.parse_pathname, *skywater_pdk.base.parse_filename*, *skywater_pdk.base.Cell*, *skywater_pdk.base.LibraryNode*, *skywater_pdk.base.LibrarySource*, *skywater_pdk.base.LibraryType*, *skywater_pdk.base.LibraryVersion*

Examples

```
>>> l = Library.parse("sky130_fd_sc_hd")
>>> l
Library(node=LibraryNode.SKY130, source=LibrarySource('fd'), type=LibraryType.sc,
↪name='hd', version=None)
>>> l.fullname
'sky130_fd_sc_hd'
>>> l.source.fullname
'The SkyWater Foundary'
>>> print(l.type)
Standard Cells
```

```
>>> l = Library.parse("sky130_rrr_sc_hd")
>>> l
Library(node=LibraryNode.SKY130, source=LibrarySource('rrr'), type=LibraryType.sc,
↪name='hd', version=None)
>>> l.fullname
'sky130_rrr_sc_hd'
>>> l.source.fullname
"Unknown source: 'rrr'"
```

```
>>> l1 = Library.parse("sky130_fd_sc_hd")
>>> l2 = Library.parse("sky130_fd_sc_hdll")
>>> l = [l2, None, l1]
>>> l.sort()
```

node: *LibraryNode*

source: *LibrarySource*

type: *LibraryType*

class skywater_pdk.base.**LibraryNode**(*value*)

> Bases: Enum
>
> Process node for a library.
>
> **SKY130 = 'SkyWater 130nm'**
>
> **classmethod parse**(*s*)
>
> **to_json**()

class skywater_pdk.base.**LibrarySource**

> Bases: str
>
> Where a library was created.
>
> **Known = [LibrarySource('fd'), LibrarySource('ef'), LibrarySource('osu')]**
>
> **property fullname**
>
> **classmethod parse**(*s*)
>
> **to_json**()

class skywater_pdk.base.**LibraryType**(*value*)

> Bases: Enum
>
> Type of library contents.
>
> **io = 'IO and Periphery'**
>
> **classmethod parse**(*s*)
>
> **pr = 'Primitives'**
>
> **sc = 'Standard Cells'**
>
> **sp = 'Build Space (Flash, SRAM, etc)'**
>
> **to_json**()
>
> **xx = 'Miscellaneous'**

class skywater_pdk.base.**LibraryVersion**(*milestone: int = 0, major: int = 0, minor: int = 0, commits: int = 0, hash: str = ''*)

> Bases: *LibraryVersion*
>
> Version number for a library.

See also:

skywater_pdk.base.LibraryNode,   *skywater_pdk.base.LibrarySource*,   *skywater_pdk.base.*
LibraryType, *skywater_pdk.base.LibraryVersion*

Examples

```
>>> v0 = LibraryVersion.parse("v0.0.0")
>>> v0
LibraryVersion(milestone=0, major=0, minor=0, commits=0, hash='')
>>> v1a = LibraryVersion.parse("v0.0.0-10-g123abc")
>>> v1a
LibraryVersion(milestone=0, major=0, minor=0, commits=10, hash='123abc')
>>> v1b = LibraryVersion.parse("v0.0.0-4-g123abc")
>>> v1b
LibraryVersion(milestone=0, major=0, minor=0, commits=4, hash='123abc')
>>> v2 = LibraryVersion.parse("v0.0.2")
>>> v2
LibraryVersion(milestone=0, major=0, minor=2, commits=0, hash='')
>>> v3 = LibraryVersion.parse("v0.2.0")
>>> v3
LibraryVersion(milestone=0, major=2, minor=0, commits=0, hash='')
>>> v4 = LibraryVersion.parse("v0.0.10")
>>> v4
LibraryVersion(milestone=0, major=0, minor=10, commits=0, hash='')
>>> v0 < v1a
True
>>> v1a < v2
True
>>> v0 < v2
True
>>> l = [v1a, v2, v3, None, v1b, v0, v2]
>>> l.sort()
>>> [i.fullname for i in l]
['0.0.0', '0.0.0-4-g123abc', '0.0.0-10-g123abc', '0.0.2', '0.0.2', '0.2.0']
```

skywater_pdk.base.**parse_filename**(*pathname*) → Tuple[*Library* | *Cell*, str | None, str | None]

Extract library and module name from filename.

> **Returns**
>
> - **obj** (*Library or Cell*) – Library or Cell information parsed from filename
>
> - **extra** (*str, optional*) – String containing any extra unparsed data (like corner information)
>
> - **ext** (*str, optional*) – String containing the file extension

See also:

skywater_pdk.base.parse_pathname, *skywater_pdk.base.Cell*, *skywater_pdk.base.Library*

Examples

```
>>> t = list(parse_filename('sky130_fd_io__top_ground_padonlyv2__tt_1p80V_3p30V_
↪3p30V_25C.wrap.lib'))
>>> t.pop(0)
Cell(name='top_ground_padonlyv2', library=Library(node=LibraryNode.SKY130,
↪source=LibrarySource('fd'), type=LibraryType.io, name='', version=None))
>>> t.pop(0)
'tt_1p80V_3p30V_3p30V_25C'
>>> t.pop(0)
'wrap.lib'
>>> t = list(parse_filename('v0.10.0/sky130_fd_sc_hdll__a211o__tt_1p80V_3p30V_3p30V_
↪25C.wrap.json'))
>>> t.pop(0)
Cell(name='a211o', library=Library(node=LibraryNode.SKY130, source=LibrarySource('fd
↪'), type=LibraryType.sc, name='hdll', version=LibraryVersion(milestone=0,
↪major=10, minor=0, commits=0, hash='')))
>>> t.pop(0)
'tt_1p80V_3p30V_3p30V_25C'
>>> t.pop(0)
'wrap.json'
```

```
>>> t = list(parse_filename('sky130_fd_io/v0.1.0/sky130_fd_io__top_powerhv_hvc_wpad_
↪_tt_1p80V_3p30V_100C.wrap.json'))
>>> t.pop(0)
Cell(name='top_powerhv_hvc_wpad', library=Library(node=LibraryNode.SKY130,
↪source=LibrarySource('fd'), type=LibraryType.io, name='',
↪version=LibraryVersion(milestone=0, major=1, minor=0, commits=0, hash='')))
>>> from skywater_pdk.corners import parse_filename as pf_corners
>>> pf_corners(t.pop(0))
(Corner(corner=(CornerType.t, CornerType.t), volts=(1.8, 3.3), temps=(100,),
↪flags=None), [])
>>> t.pop(0)
'wrap.json'
```

```
>>> parse_filename('libraries/sky130_fd_io/v0.2.1/cells/analog_pad/sky130_fd_io-
↪analog_pad.blackbox.v')[0]
Cell(name='analog_pad', library=Library(node=LibraryNode.SKY130,
↪source=LibrarySource('fd'), type=LibraryType.io, name='',
↪version=LibraryVersion(milestone=0, major=2, minor=1, commits=0, hash='')))
```

```
>>> t = list(parse_filename('skywater-pdk/libraries/sky130_fd_sc_hd/v0.0.1/cells/
↪a2111o/sky130_fd_sc_hd__a2111o.blackbox.v'))
>>> t.pop(0)
Cell(name='a2111o', library=Library(node=LibraryNode.SKY130, source=LibrarySource(
↪'fd'), type=LibraryType.sc, name='hd', version=LibraryVersion(milestone=0,
↪major=0, minor=1, commits=0, hash='')))
>>> assert t.pop(0) is None
>>> t.pop(0)
'blackbox.v'
```

skywater_pdk.base.**parse_pathname**(*pathname*)

    Extract library and module name for pathname.

Returns

- **obj** (*Library or Cell*) – Library or Cell information parsed from filename
- **filename** (*str, optional*) – String containing any filename extracted. String containing the file extension

See also:

skywater_pdk.base.parse_filename, *skywater_pdk.base.Cell*, *skywater_pdk.base.Library*

Examples

```
>>> parse_pathname('skywater-pdk/libraries/sky130_fd_sc_hd/v0.0.1/cells/a2111o')
(Cell(name='a2111o', library=Library(node=LibraryNode.SKY130, source=LibrarySource(
→'fd'), type=LibraryType.sc, name='hd', version=LibraryVersion(milestone=0,
→major=0, minor=1, commits=0, hash=''))), None)
```

```
>>> parse_pathname('skywater-pdk/libraries/sky130_fd_sc_hd/v0.0.1/cells/a2111o/
→README.rst')
(Cell(name='a2111o', library=Library(node=LibraryNode.SKY130, source=LibrarySource(
→'fd'), type=LibraryType.sc, name='hd', version=LibraryVersion(milestone=0,
→major=0, minor=1, commits=0, hash=''))), 'README.rst')
```

```
>>> parse_pathname('skywater-pdk/libraries/sky130_fd_sc_hd/v0.0.1')
(Library(node=LibraryNode.SKY130, source=LibrarySource('fd'), type=LibraryType.sc,
→name='hd', version=LibraryVersion(milestone=0, major=0, minor=1, commits=0, hash='
→')), None)
```

```
>>> parse_pathname('skywater-pdk/libraries/sky130_fd_sc_hd/v0.0.1/README.rst')
(Library(node=LibraryNode.SKY130, source=LibrarySource('fd'), type=LibraryType.sc,
→name='hd', version=LibraryVersion(milestone=0, major=0, minor=1, commits=0, hash='
→')), 'README.rst')
```

```
>>> parse_pathname('libraries/sky130_fd_sc_hd/v0.0.1')
(Library(node=LibraryNode.SKY130, source=LibrarySource('fd'), type=LibraryType.sc,
→name='hd', version=LibraryVersion(milestone=0, major=0, minor=1, commits=0, hash='
→')), None)
```

```
>>> parse_pathname('libraries/sky130_fd_sc_hd/v0.0.1/README.rst')
(Library(node=LibraryNode.SKY130, source=LibrarySource('fd'), type=LibraryType.sc,
→name='hd', version=LibraryVersion(milestone=0, major=0, minor=1, commits=0, hash='
→')), 'README.rst')
```

```
>>> parse_pathname('sky130_fd_sc_hd/v0.0.1')
(Library(node=LibraryNode.SKY130, source=LibrarySource('fd'), type=LibraryType.sc,
→name='hd', version=LibraryVersion(milestone=0, major=0, minor=1, commits=0, hash='
→')), None)
```

```
>>> parse_pathname('sky130_fd_sc_hd/v0.0.1/README.rst')
(Library(node=LibraryNode.SKY130, source=LibrarySource('fd'), type=LibraryType.sc,
→name='hd', version=LibraryVersion(milestone=0, major=0, minor=1, commits=0, hash='
→')), 'README.rst')
```

```
>>> parse_pathname('sky130_fd_sc_hd/v0.0.1/RANDOM')
(Library(node=LibraryNode.SKY130, source=LibrarySource('fd'), type=LibraryType.sc,␣
↪name='hd', version=LibraryVersion(milestone=0, major=0, minor=1, commits=0, hash='
↪')), 'RANDOM')
```

```
>>> parse_pathname('RANDOM')
Traceback (most recent call last):
    ...
ValueError: ...
```

```
>>> parse_pathname('libraries/RANDOM/v0.0.1')
Traceback (most recent call last):
    ...
ValueError: ...
```

```
>>> parse_pathname('libraries/skywater_fd_sc_hd/vA.B.C')
Traceback (most recent call last):
    ...
ValueError: ...
```

11.1.3 skywater_pdk.corners module

class skywater_pdk.corners.**Corner**(*corner: Tuple[*CornerType*, *CornerType*], volts: Tuple[float, ...], temps: Tuple[int, ...], flags: Tuple[*CornerFlag*, ...] | None = None*)

Bases: *Corner*

See also:

skywater_pdk.corners.parse_filename, *skywater_pdk.base.Cell*, *skywater_pdk.corners.CornerType*, *skywater_pdk.corners.CornerFlag*

corner: Tuple[*CornerType*, *CornerType*]

temps: Tuple[int, ...]

volts: Tuple[float, ...]

class skywater_pdk.corners.**CornerFlag**(*value*)

Bases: *OrderedFlag*

See also:

skywater_pdk.corners.Corner, *skywater_pdk.corners.CornerType*

ccsnoise = 'Composite Current Source Noise'

hv = 'High voltage'

lowhv = 'Low High Voltage'

lv = 'Low voltage'

nointpr = 'No internal power'

classmethod parse(*s*)

pwr = 'Power'

to_json()

w = 'w'

xx = 'xx'

class skywater_pdk.corners.**CornerType**(*value*)

    Bases: *OrderedFlag*

    See also:

    skywater_pdk.corners.Corner, *skywater_pdk.corners.CornerFlag*

    Examples

```
>>> CornerType.parse('t')
CornerType.t
>>> CornerType.parse('tt')
[CornerType.t, CornerType.t]
>>> CornerType.parse('wp')
[CornerType.f, CornerType.f]
```

    f = 'Fast'

    classmethod parse(*s*)

    s = 'Slow'

    t = 'Typical'

    to_json()

class skywater_pdk.corners.**OptionalTuple**(*iterable=(), /*)

    Bases: *OptionalTuple*

skywater_pdk.corners.**parse_filename**(*pathname*)

    Extract corner information from a filename.

    See also:

    skywater_pdk.base.parse_pathname, skywater_pdk.base.parse_filehname

    Examples

```
>>> parse_filename('tt_1p80V_3p30V_3p30V_25C')
(Corner(corner=(CornerType.t, CornerType.t), volts=(1.8, 3.3, 3.3), temps=(25,),
↪flags=None), [])
```

```
>>> parse_filename('sky130_fd_io__top_ground_padonlyv2__tt_1p80V_3p30V_3p30V_25C.
↪wrap.lib')
(Corner(corner=(CornerType.t, CornerType.t), volts=(1.8, 3.3, 3.3), temps=(25,),
↪flags=None), [])
```

```
>>> parse_filename('sky130_fd_sc_ms__tt_1p80V_100C.wrap.json')
(Corner(corner=(CornerType.t, CornerType.t), volts=(1.8,), temps=(100,),
→flags=None), [])
```

```
>>> parse_filename('sky130_fd_sc_ms__tt_1p80V_100C.wrap.lib')
(Corner(corner=(CornerType.t, CornerType.t), volts=(1.8,), temps=(100,),
→flags=None), [])
```

```
>>> parse_filename('sky130_fd_sc_ms__tt_1p80V_25C_ccsnoise.wrap.json')
(Corner(corner=(CornerType.t, CornerType.t), volts=(1.8,), temps=(25,),
→flags=(CornerFlag.ccsnoise,)), [])
```

```
>>> parse_filename('sky130_fd_sc_ms__wp_1p65V_n40C.wrap.json')
(Corner(corner=(CornerType.f, CornerType.f), volts=(1.65,), temps=(-40,),
→flags=None), [])
```

```
>>> parse_filename('sky130_fd_sc_ms__wp_1p95V_85C_pwr.wrap.lib')
(Corner(corner=(CornerType.f, CornerType.f), volts=(1.95,), temps=(85,),
→flags=(CornerFlag.pwr,)), [])
```

```
>>> parse_filename('sky130_fd_sc_ms__wp_1p95V_n40C_ccsnoise.wrap.json')
(Corner(corner=(CornerType.f, CornerType.f), volts=(1.95,), temps=(-40,),
→flags=(CornerFlag.ccsnoise,)), [])
```

```
>>> parse_filename('sky130_fd_sc_ms__wp_1p95V_n40C_pwr.wrap.lib')
(Corner(corner=(CornerType.f, CornerType.f), volts=(1.95,), temps=(-40,),
→flags=(CornerFlag.pwr,)), [])
```

```
>>> parse_filename('sky130_fd_sc_hd__a2111o_4__ss_1p76V_n40C.cell.json')
(Corner(corner=(CornerType.s, CornerType.s), volts=(1.76,), temps=(-40,),
→flags=None), [])
```

```
>>> parse_filename('sky130_fd_sc_ls__lpflow_lsbuf_lh_1__lpflow_wc_lh_level_shifters_
→ss_1p95V_n40C.cell.json')
(Corner(corner=(CornerType.s, CornerType.s), volts=(1.95,), temps=(-40,),
→flags=None), ['wc', 'lh', 'level', 'shifters'])
```

```
>>> parse_filename('sky130_fd_sc_hvl__lsbufhv2hv_hl_1__ff_5p50V_lowhv_1p65V_lv_ss_
→1p60V_100C.cell.json')
(Corner(corner=(CornerType.f, CornerType.s), volts=(5.5, 1.65, 1.6), temps=(100,),
→flags=(CornerFlag.lowhv, CornerFlag.lv)), [])
```

11.1.4 skywater_pdk.sizes module

class skywater_pdk.sizes.`CellSize`

> Bases: `ABC`
>
> Drive strength variants of a given cell.
>
> **See also:**
>
> *skywater_pdk.base.Cell*, *skywater_pdk.sizes.CellSizeNumeric*, *skywater_pdk.sizes.CellSizeLowPower*, *skywater_pdk.sizes.CellSizeMinimum*
>
> **Examples**
>
> ```
> >>> d1 = CellSize.from_suffix("_1")
> >>> d2 = CellSize.from_suffix("_lp")
> >>> d3 = CellSize.from_suffix("_m")
> >>> d4 = CellSize.from_suffix("_2")
> >>> CellSize.from_suffix("_abc")
> Traceback (most recent call last):
>     ...
> InvalidSuffixError: Invalid suffix: _abc
> >>> l = [d1, d2, d3, d4]
> >>> l
> [CellSizeNumeric(units=1), CellSizeLowPower(lp_variant=0), CellSizeMinimum(),
> ↪CellSizeNumeric(units=2)]
> >>> l.sort()
> >>> l
> [CellSizeNumeric(units=1), CellSizeNumeric(units=2), CellSizeLowPower(lp_variant=0),
> ↪ CellSizeMinimum()]
> ```
>
> **abstract** `describe`()
>
> **classmethod** `from_suffix`(*s*)
>
> **abstract property** `suffix`

class skywater_pdk.sizes.`CellSizeLowPower`(*lp_variant: int = 0*)

> Bases: *CellSize*
>
> **See also:**
>
> *skywater_pdk.base.Cell*, *skywater_pdk.sizes.CellSize*, *skywater_pdk.sizes.CellSizeNumeric*, *skywater_pdk.sizes.CellSizeMinimum*
>
> **Examples**
>
> ```
> >>> lp = CellSizeLowPower.from_suffix("_lp")
> >>> lp2 = CellSizeLowPower.from_suffix("_lp2")
> >>> lp3 = CellSizeLowPower.from_suffix("_lp3")
> >>> CellSizeLowPower.from_suffix("_ld")
> Traceback (most recent call last):
>     ...
> InvalidSuffixError: Invalid suffix: _ld
> ```

```
>>> lp
CellSizeLowPower(lp_variant=0)
>>> lp2
CellSizeLowPower(lp_variant=1)
>>> lp3
CellSizeLowPower(lp_variant=2)
>>> str(lp)
'with size for low power'
>>> str(lp2)
'with size for low power (alternative)'
>>> str(lp3)
'with size for low power (extra alternative 0)'
>>> lp.describe()
'for low power'
>>> lp2.describe()
'for low power (alternative)'
>>> lp3.describe()
'for low power (extra alternative 0)'
>>> lp.suffix
'_lp'
>>> lp2.suffix
'_lp2'
>>> lp3.suffix
'_lp3'
```

describe()

classmethod **from_dict**(*kvs: dict | list | str | int | float | bool | None, *, infer_missing=False*) → A

classmethod **from_json**(*s: str | bytes | bytearray, *, parse_float=None, parse_int=None, parse_constant=None, infer_missing=False, **kw*) → A

classmethod **from_suffix**(*s*)

lp_variant: int = 0

classmethod **schema**(*, *infer_missing: bool = False, only=None, exclude=(), many: bool = False, context=None, load_only=(), dump_only=(), partial: bool = False, unknown=None*) → SchemaF[A]

property suffix

to_dict(*encode_json=False*) → Dict[str, dict | list | str | int | float | bool | None]

to_json(*, *skipkeys: bool = False, ensure_ascii: bool = True, check_circular: bool = True, allow_nan: bool = True, indent: int | str | None = None, separators: Tuple[str, str] | None = None, default: Callable | None = None, sort_keys: bool = False, **kw*) → str

class skywater_pdk.sizes.**CellSizeMinimum**

Bases: *CellSize*

See also:

skywater_pdk.base.Cell, *skywater_pdk.sizes.CellSize*, *skywater_pdk.sizes.CellSizeNumeric*, *skywater_pdk.sizes.CellSizeLowPower*

Examples

```
>>> m = CellSizeMinimum.from_suffix("_m")
>>> CellSizeMinimum.from_suffix("_m2")
Traceback (most recent call last):
    ...
InvalidSuffixError: Invalid suffix: _m2
>>> m
CellSizeMinimum()
>>> str(m)
'with size minimum'
>>> m.describe()
'minimum'
>>> m.suffix
'_m'
```

```
>>> m1 = CellSizeMinimum()
>>> m2 = CellSizeMinimum()
>>> assert m1 is m2
```

describe()

classmethod from_suffix(*s*)

property suffix

to_dict()

class skywater_pdk.sizes.**CellSizeNumeric**(*units: int*)

Bases: *CellSize*

See also:

skywater_pdk.base.Cell, *skywater_pdk.sizes.CellSize*, *skywater_pdk.sizes.CellSizeLowPower*, *skywater_pdk.sizes.CellSizeMinimum*

Examples

```
>>> s1 = CellSizeNumeric.from_suffix("_1")
>>> s2 = CellSizeNumeric.from_suffix("_2")
>>> s3 = CellSizeNumeric.from_suffix("_3")
>>> CellSizeNumeric.from_suffix("_-1")
Traceback (most recent call last):
    ...
InvalidSuffixError: Invalid suffix: _-1
>>> s1
CellSizeNumeric(units=1)
>>> s2
CellSizeNumeric(units=2)
>>> s3
CellSizeNumeric(units=3)
>>> str(s1)
'with size of 1 units'
```

```
>>> str(s2)
'with size of 2 units'
>>> str(s3)
'with size of 3 units (invalid?)'
>>> s1.describe()
'of 1 units'
>>> s2.describe()
'of 2 units'
>>> s3.describe()
'of 3 units (invalid?)'
>>> s1.suffix
'_1'
>>> s2.suffix
'_2'
>>> s3.suffix
'_3'
```

VALID_UNIT_VALUES = (0, 1, 2, 4, 8, 6, 12, 14, 16, 20, 32)

describe()

classmethod from_dict(*kvs: dict | list | str | int | float | bool | None, *, infer_missing=False*) → A

classmethod from_json(*s: str | bytes | bytearray, *, parse_float=None, parse_int=None, parse_constant=None, infer_missing=False, **kw*) → A

classmethod from_suffix(*s*)

classmethod schema(**, infer_missing: bool = False, only=None, exclude=(), many: bool = False, context=None, load_only=(), dump_only=(), partial: bool = False, unknown=None*) → SchemaF[A]

property suffix

to_dict(*encode_json=False*) → Dict[str, dict | list | str | int | float | bool | None]

to_json(**, skipkeys: bool = False, ensure_ascii: bool = True, check_circular: bool = True, allow_nan: bool = True, indent: int | str | None = None, separators: Tuple[str, str] | None = None, default: Callable | None = None, sort_keys: bool = False, **kw*) → str

units: int

exception skywater_pdk.sizes.**InvalidSuffixError**(*s*)

    Bases: ValueError

skywater_pdk.sizes.**parse_size**(*s*)

```
>>> parse_size('_1')
CellSizeNumeric(units=1)
```

```
>>> parse_size('a2111o_1')
CellSizeNumeric(units=1)
```

```
>>> parse_size('sky130_fd_sc_ms__sdfrtp_1.v')
CellSizeNumeric(units=1)
```

```
>>> parse_size('libraries/sky130_fd_sc_ms/v0.0.1/cells/sdfrtp/sky130_fd_sc_ms__
→sdfrtp_1.v')
CellSizeNumeric(units=1)
```

```
>>> parse_size('libraries/sky130_fd_sc_ms/v0.0.1/cells/sdfrtp/sky130_fd_sc_ms__
→sdfrtp_1.bb.blackbox.v')
CellSizeNumeric(units=1)
```

```
>>> parse_size('libraries/sky130_fd_sc_ms/v0.0.1/cells/sdfrtp/sky130_fd_sc_ms__
→sdfrtp.v')
>>> parse_size('sky130_fd_sc_ms__sdfrtp.v')
>>> parse_size('_blah')
```

11.1.5 skywater_pdk.utils module

class skywater_pdk.utils.**OrderedFlag**(*value*)

> Bases: `Flag`
>
> An enumeration.

skywater_pdk.utils.**comparable_to_none**(*cls*)

Examples

```
>>> @comparable_to_none
... @dataclass(order=True)
... class A:
...     a: int = 0
>>> @comparable_to_none
... @dataclass(order=True)
... class B:
...     b: Optional[A] = None
>>> b0 = B()
>>> repr(b0)
'B(b=None)'
>>> str(b0)
'B(b=None)'
>>> b1 = B(A())
>>> repr(b1)
'B(b=A(a=0))'
>>> str(b1)
'B(b=A(a=0))'
>>> b2 = B(A(2))
>>> repr(b2)
'B(b=A(a=2))'
>>> str(b2)
'B(b=A(a=2))'
>>> l = [b0, b1, b2, None]
>>> for i in range(0, 3):
...     random.shuffle(l)
```

```
...     l.sort()
...     print(l)
[None, B(b=None), B(b=A(a=0)), B(b=A(a=2))]
[None, B(b=None), B(b=A(a=0)), B(b=A(a=2))]
[None, B(b=None), B(b=A(a=0)), B(b=A(a=2))]
```

skywater_pdk.utils.**dataclass_json_passthru_config**(*args*, ***kw*)

skywater_pdk.utils.**dataclass_json_passthru_sequence_config**(*args*, ***kw*)

skywater_pdk.utils.**extract_numbers**(*s*)

> Create tuple with sequences of numbers converted to ints.

```
>>> extract_numbers("pwr_template13x10")
('pwr_template', 13, 'x', 10)
>>> extract_numbers("vio_10_10_1")
('vio_', 10, '_', 10, '_', 1)
```

skywater_pdk.utils.**sortable_extracted_numbers**(*s*)

> Create output which is sortable by numeric values in string.

```
>>> sortable_extracted_numbers("pwr_template13x10")
('pwr_template', '0000000013', 'x', '0000000010')
>>> sortable_extracted_numbers("vio_10_10_1")
('vio_', '0000000010', '_', '0000000010', '_', '0000000001')
```

```
>>> l = ['a1', 'a2b2', 'a10b10', 'b2', 'a8b50', 'a10b1']
>>> l.sort()
>>> print('\n'.join(l))
a1
a10b1
a10b10
a2b2
a8b50
b2
>>> l.sort(key=sortable_extracted_numbers)
>>> print('\n'.join(l))
a1
a2b2
a8b50
a10b1
a10b10
b2
```

11.1.6 Module contents

PREVIOUS NOMENCLATURE

During the process of preparing the SkyWater SKY130 PDK for public release, consistency around naming, documentation and data cross checking was performed. This attempted to make sure that all references have been updated but despite the SkyWater PDK Author's best efforts, some references may have been missed.

This section of the document include information about previous nomenclature around both the SkyWater PDK, related process and technologies developed both by Cypress Technology, SkyWater Technology and their partners.

Note: If you find any references to these terms inside the current documentation, please create an issue so we can update the documentation!

This section should also help people who have previously had access (under NDA) to Cypress and SkyWater PDK files or older documentation and want to migrate to this new open source PDK.

Warning: Despite this repository being released under an open source license, you should **not** publish publically any Cypress or SkyWater IP you have been given access to under NDA.

If the IP you are looking at includes references to terms found in this Previous Nomenclature section, it is a good indication that the IP you have can only be shared under appropriate NDAs and clearances you should **not** be publically publishing it.

---

s8
> The old Cypress and SkyWater name for the SKY130 process. It stood for the "8th generation" of the SONOS technology developed originally by Cypress.

s180
> The name for using 180nm technology on the 130nm process.

s8pfhd
> The base process. 5 metal layer backend stack, 16V devices, deep nwell.

s8phirs
> The base process plus rdl layer and rdl metal inductors.

s8phrc
> The base process plus dual MiM cap layers on metal 3 and metal 4

s8pfn-20
> The base process plus UHV (ultra-high voltage) implants for 20V device support.

s8iom0s8
> An earlier name for the sky130_fd_io library.

scs8hd
> An earlier name for the sky130_fd_sc_hd library.

GLOSSARY

SkyWater
SkyWater Technology
> SkyWater Technology

Cypress
Cypress Technologies
> Cypress Technologies

Linear ASICs
> Linear ASICs

Mentor
Mentor Graphics
> Mentor, a Siemens Business is a US-based electronic design automation (EDA) multinational corporation for electrical engineering and electronics.

OSU
> Oklahoma State University

VSD
VLSI System Design
> VLSI System Design

sc
Standard Cell
> The basic building blocks of digital circuit design.

ce
> Memory Core

Antenna Rule Violations
> During manufacturing, a static charge can build up on the currently- topmost metal layer, and destroy the chip if there is no path to the substrate for this charge to bleed off during layer deposition. The Antenna Rule ensures that each metal layer has a route to diffusion.

CIF
Caltech Intermediate Form
> From the 1990's, the CIF format has largely been replaced by the GDS format.

CCS
ECSM
> Current Source Models

DRC
Design Rule Check
Design Rule Checking
> Design rule checking or check(s) is the process of determing whether the physical layout of a particular chip

layout satisfies a series of required parameters called design rules.

ESD
Electro-Static Discharge (protection from)
    Circuit elements, especially on I/O pins, intended to protect the circuit from the effects of electrostatic discharge.

LVS
Layout Verse Schematic
    Layout Versus Schematic (LVS) verification is the process of determining whether a particular integrated circuit layout corresponds to the original schematic or circuit diagram of the design.

MiM
MIM
MiM caps
    Stands for "metal-insulator-metal" and is a type of IC capacitor structure.

    These are capacitors that are made between two metal route layers, usually close to the top of the metal stack.

    Generally they are around 1fF/um^2, a lot better than MoM caps.

    The capacitance of MiM caps is on the top and bottom of the metal (while the capacitance of MoM caps is sidewall cap).

MoM
MoM caps
VPP
VPP capacitor
    Stands for "metal-oxide-metal" and is a type of IC capacitor structure.

    These are capacitors which are made by interleaving fingers of metal.

    Sometimes MoM caps are referred to as "VPP" capacitors (stands for "vertical parallel plate").

    The capacitance of MoM caps is capacitance of the metal sidewalls which is significantly lower than that provided MiM caps.

NLDM
    Non-Linear Delay Model

OPHW
OPen HardWare
    The movement to produce inspectable and modifiable computer hardware designs.

PEX
Parasitic Extraction
    Parasitic extraction is calculation of the parasitic effects in both the designed devices and the required wiring interconnects of an electronic circuit. This includes all parasitic components (often called parasitic devices) including parasitic;

    - capacitances,

    - resistances, and

    - inductances.

PNR
Place aNd Route
    The process of laying out the standard design cells on the 2D plane of the chip and connecting their corresponding inputs and outputs. Theoretically equivalent to the "Travelling Salesman Problem," and therefore the subject of much research.

STA
Static Timing Analysis
> Analysing the timing of a circuit from some level of the design. Contrast with performing the timing analysis on actual hardware.

RTL
Register Transfer Language
> A source code format that describes the transitions that hardware registers take at the register transfer level, such as Verilog or VHDL.

VLSI
Very Large Scale Integration
> Producing an integrated circuit in the million+ transistor scale, with multiple functions on the same chip (such as compute, memory, ROM, and power regulation).

.lef
LEF
Library Exchange Format
> Abstract description of the layout for place and route.

.lib
Liberty Models
Liberty Timing Models
Liberty Wire Load Models
> Liberty Files are a IEEE Standard for defining: PVT Characterization, Relating Input and Output Characteristics, Timing, Power, Noise.
>
> Wire Load Models estimate the parasitics based on the fanout of a net.

CALMA
Calma
Calma Format
> Calma was the company behind the development of GDS. https://en.wikipedia.org/wiki/Calma

Mentor Calibre
> The Calibre® product suite developed by *Mentor Graphics*. Heavily used for IC Verification and Signoff.

MAGIC
> MAGIC

ngspice
> ngspice

OpenRoad
> The digital design flow developed by The OpenRoad Project

qflow
> qflow Named after Steve Beccue of MultiGIG.

yosys
> Yosys Open SYnthesis Suite

s8phirs_10r
SkyWater S8
SkyWater SKY130 technology
SkyWater SKY130 process
> The SkyWater SKY130 130nm process with 5 metal layers.

s8_osu130
> The Oklahoma State University Digital Standard Cells.

s8_schd
    The SkyWater High Density Digital Standard Cells.

license
Apache 2.0 license
    The Apache 2.0 license.

FOURTEEN

HOW TO CONTRIBUTE

We'd love to accept your patches and contributions to this project. There are just a few small guidelines you need to follow.

14.1 Contributor License Agreement

Contributions to this project must be accompanied by a Contributor License Agreement. You (or your employer) retain the copyright to your contribution; this simply gives us permission to use and redistribute your contributions as part of the project. Head over to https://cla.developers.google.com/ to see your current agreements on file or to sign a new one.

You generally only need to submit a CLA once, so if you've already submitted one (even if it was for a different project), you probably don't need to do it again.

14.2 Code reviews

All submissions, including submissions by project members, require review. We use GitHub pull requests for this purpose. Consult GitHub Help for more information on using pull requests.

14.3 Community Guidelines

This project follows Google's Open Source Community Guidelines.

At Google, we recognize and celebrate the creativity and collaboration of open source contributors and the diversity of skills, experiences, cultures, and opinions they bring to the projects and communities they participate in.

Every one of Google's open source projects and communities are inclusive environments, based on treating all individuals respectfully, regardless of gender identity and expression, sexual orientation, disabilities, neurodiversity, physical appearance, body size, ethnicity, nationality, race, age, religion, or similar personal characteristic.

We value diverse opinions, but we value respectful behavior more.

Respectful behavior includes:

- Being considerate, kind, constructive, and helpful.

- Not engaging in demeaning, discriminatory, harassing, hateful, sexualized, or physically threatening behavior, speech, and imagery.

- Not engaging in unwanted physical contact.

Some Google open source projects may adopt an explicit project code of conduct, which may have additional detailed expectations for participants. Most of those projects will use our modified Contributor Covenant.

14.3.1 Resolve peacefully

We do not believe that all conflict is necessarily bad; healthy debate and disagreement often yields positive results. However, it is never okay to be disrespectful.

If you see someone behaving disrespectfully, you are encouraged to address the behavior directly with those involved. Many issues can be resolved quickly and easily, and this gives people more control over the outcome of their dispute. If you are unable to resolve the matter for any reason, or if the behavior is threatening or harassing, report it. We are dedicated to providing an environment where participants feel welcome and safe.

14.3.2 Reporting problems

Some Google open source projects may adopt a project-specific code of conduct. In those cases, a Google employee will be identified as the Project Steward, who will receive and handle reports of code of conduct violations. In the event that a project hasn't identified a Project Steward, you can report problems by emailing opensource@google.com.

We will investigate every complaint, but you may not receive a direct response. We will use our discretion in determining when and how to follow up on reported incidents, which may range from not taking action to permanent expulsion from the project and project-sponsored spaces. We will notify the accused of the report and provide them an opportunity to discuss it before any action is taken. The identity of the reporter will be omitted from the details of the report supplied to the accused. In potentially harmful situations, such as ongoing harassment or threats to anyone's safety, we may take action without notice.

This document was adapted from the IndieWeb Code of Conduct *and can also be found at* <https://opensource.google/conduct/>.

PARTNERS

15.1 Open Source SkyWater PDK

15.2 Open Source MPW Shuttle Program

15.3 Industry partners

15.4 Academic partners

THE AMERICAN
UNIVERSITY IN CAIRO

Ohio Supercomputer Center
An OH·TECH Consortium Member

UC SANTA CRUZ

UC San Diego

SIXTEEN

REFERENCES

SEVENTEEN

WELCOME TO SKYWATER SKY130 PDK'S DOCUMENTATION!

Warning: This documentation is currently a **work in progress**.

EIGHTEEN

CURRENT STATUS - EXPERIMENTAL PREVIEW

> **Warning:**   Google and SkyWater are currently treating the current content as an **experimental preview / alpha release**.

While the SKY130 process node and the PDK from which this open source release was derived have been used to create many designs that have been successfully manufactured commercially in significant quantities, the open source PDK is not intended to be used for production settings at this current time. It *should* be usable for doing test chips and initial design verification (but this is not guaranteed).

Google, SkyWater and our partners are currently doing internal validation and test designs, including silicon validation or the released data and plan to publish these results.

The PDK will be tagged with a production version when ready to do production design, see the "*Versioning Information*" section for a full description of the version numbering scheme.

To get notified about future new releases of the PDK, and other important news, please sign up on the skywater-pdk-announce mailing list [join link].

RESOURCES

The latest SkyWater SKY130 PDK design resources can be downloaded from the following repositories:

- On Github @ google/skywater-pdk

- Google CodeSearch interface @ https://cs.opensource.google/skywater-pdk

- foss-eda-tools.googlesource.com/skywater-pdk

INDICES AND TABLES

- *Glossary*
- genindex
- modindex
- search

BIBLIOGRAPHY

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